ZnO-based nonvolatile memory thin-film transistors with polymer dielectric/ferroelectric double gate insulators

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The authors report on the fabrication of a top-gate ZnO thin-film transistor (TFT) with a polymer dielectric/ferroelectric double-layer gate insulator that was formed on patterned ZnO through a sequential spin-casting process of 450-nm-thick poly-4-vinylphenol (PVP) and 200-nm-thick poly(vinylidene fluoride/trifluoroethylene) [P(VDF/TrFE)]. Compared to the single P(VDF/TrFE) layer, double layer shows remarkably reduced leakage current with the aid of the PVP buffer. TFT with the PVP/P(VDF/TrFE) double layer exhibits a field effect mobility of 0.36 cm^2/V and a large memory hysteresis in the transfer characteristics due to the ferroelectric P(VDF/TrFE). The retention of the device lasted over 2 h. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2749841]

Field effect transistors with ferroelectric gate insulators (FeFETs) have been extensively researched because of their nonvolatile memory retention and nondestructive readout.[1,2] Their memory effect originates from the ferroelectric polarization of the gate insulator which leads to modulation of the channel conductance. Inorganic materials such as lead zirconate titanate[3] and strontium bismuth tantalate[4] have been the focused materials for Si-based FeFET, requiring very high process temperatures (usually above 500 °C) for good ferroelectric properties. Very recently, researchers study organic thin-film materials for the nonvolatile memory (NVM) applications, desiring the memory to be realized on plastic or glass substrates.[5,6] Poly(vinylidene fluoride/trifluoroethylene) [P(VDF/TrFE)] copolymer is one of the attractive ferroelectric polymers for the NVM applications since it has a high remnant polarization ($\sim 11.9\ \mu C/cm^2$),[7] short switching time (~ 1 ms),[8] and ease of fabrication in thin-film form by the solution process at a low temperature. However, the P(VDF/TrFE) film usually shows large gate leakage current which deteriorates the performance of the FeFETs because TrFE in the middle of the chain can act as a leakage path.[7] In the present study, we have fabricated ZnO-based top-gate FeFETs which show a large memory window and good data retention properties without serious gate leakage current, inserting an additional poly-4-vinylphenol (PVP) layer between the P(VDF/TrFE) layer and the active layer. Adopting inorganic ZnO channel, we could thus obtain the high value of field effect mobility as well.

The glass (Corning 1737) substrate was cleaned with acetone, methanol, and de-ionized water, in that order. Then 150-nm-thick ZnO films were deposited at a low substrate temperature of 100 °C by rf sputtering in a vacuum chamber (with base pressure of 1×10^{-6} and working pressure of 10 mTorr composed of the mixture of $Ar:O_2=6:1$), and then Al source/drain electrodes were patterned by thermal evaporation. Spin casting was performed to cover the patterned ZnO structure with 450-nm-thick PVP layer, followed by a curing process at 175 °C for 1 h in vacuum. Then, a 200-nm-thick film of P(VDF/TrFE) 75/25 mol % copolymer was also coated by spin casting 6 wt % cyclohexanone solutions and was cured at 135 °C for 2 h in air. Finally, Al top-gate electrode was deposited by thermal evaporation. Figure 1(a) shows a schematic cross section of our device, which has a nominal channel length (L) of 90 μm and a width/length (W/L) ratio of ~ 6.

All current-voltage (I-V) or current density–electric field (J-E) characterizations were carried out with a semiconductor parameter analyzer (model HP 4155C, Agilent Technologies) in the dark at room temperature. Capacitance-voltage (C-V) measurements were performed with a C-V meter (model HP 4284A, Agilent Technologies). Film thickness was determined by a surface profiler (Alpha-Step IQ).

Figure 1(b) shows the capacitance-voltage (C-V) and current density–electric field (J-E) (inset) characteristics of ferroelectric P(VDF/TrFE) single insulator (200 nm thick), while Fig. 1(c) displays those characteristics of our PVP (450-nm-thick dielectric)/P(VDF/TrFE) (200-nm-thick ferroelectric) double insulator as obtained from 300 μm diameter Al/insulator/indium tin oxide structure. During the voltage sweeps from −20 to 20 V and vice versa, the capacitance of the 200-nm-thick P(VDF/TrFE) film varied from 30.2 to 42.9 nF/cm^2 showing the same peak value near −9 and 9 V. According to the capacitance data, the dielectric constant k_{FE} of the P(VDF/TrFE) film was estimated to be 6.8–9.7. The peaks of J-E curve also appeared at the same voltages, which shows the ferroelectric switching behavior of the P(VDF/TrFE) film due to the displacement current. From the peak positions of the C-V and J-E curves, the coercive field (E_c) of our P(VDF/TrFE) film was determined to be 0.45 MV/cm. Then, based on the coercive field of P(VDF/TrFE) and the following equation,[9] we could work out the coercive voltage (V_c) for 450-nm-thick PVP/200-nm-thick P(VDF/TrFE) double layer.

$$V_c^{\text{double layer}} = E_c^{\text{FE}} \frac{k_i t_{\text{FE}} + k_{\text{FE}} t_i}{k_i}, \tag{1}$$

where $k_i(\sim 4.0)$ and k_{FE} (~ 9.7 for switching event) are the measured dielectric constants of the PVP and P(VDF/TrFE)

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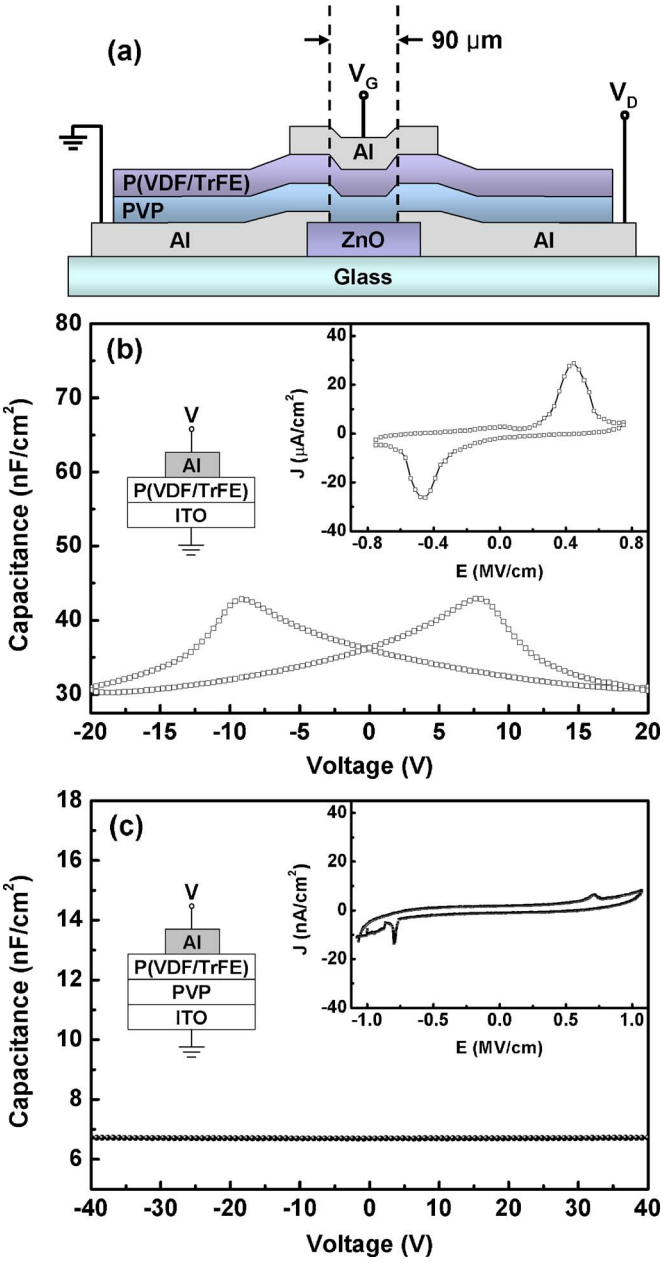

FIG. 1. (Color online) (a) Schematic cross section of our top-gate ZnO-FeFET with 450-nm-thick PVP/200-nm-thick P(VDF/TrFE) double insulator. (b) Capacitance-voltage (*C-V*) and the current density–electric field (*J-E*) (inset) characteristics of 200-nm-thick P(VDF/TrFE) single layer. (c) Capacitance-voltage (*C-V*) and the current density–electric field (*J-E*) (inset) characteristics of the PVP/P(VDF/TrFE) double layer.

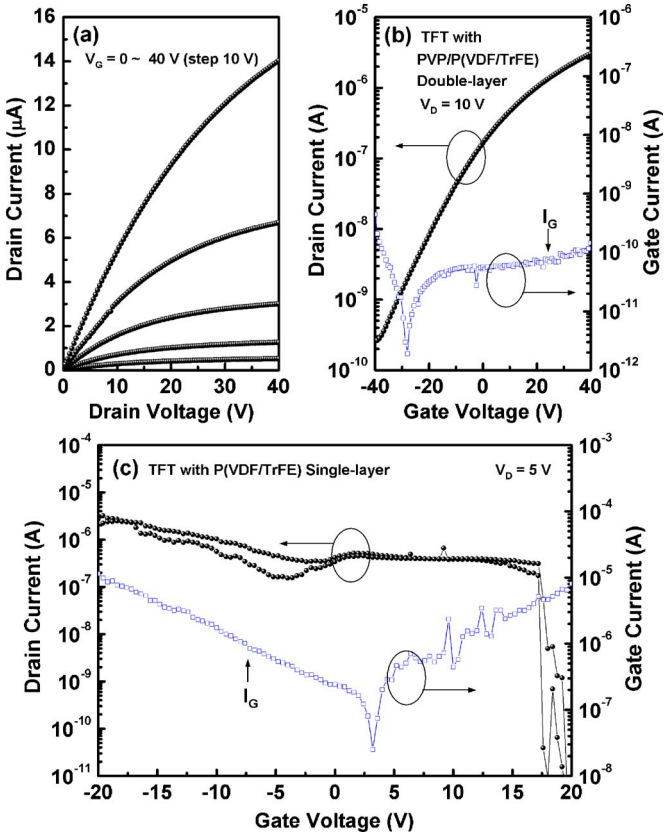

FIG. 2. (Color online) (a) I_D-V_D output and (b) I_D-V_G transfer characteristics obtained from the FeFET with PVP/P(VDF/TrFE) double layer in the pristine state. (c) I_D-V_G transfer characteristics of the device with single P(VDF/TrFE) layer.

films, respectively, while t_i and t_{FE} are their respective thicknesses. The V_c value was then estimated to be ±57 V which is relatively close to our experimental peak positions (±51 V or ~±0.8 MV/cm) [see the *J-E* curve in the inset of Fig. 1(c)]. We could not observe the switching behavior of the double layer in the *C-V* measurement, partly because the allowed voltage scan range of our *C-V* meter was limited to ±40 V which is well below 51 V, but mainly because the thick PVP layer significantly reduces the total capacitance value so that the switching event may not easily be detected in our double layer. While much higher capacitance was achieved from the single P(VDF/TrFE) layer, it also showed three orders of magnitude higher leakage current density than that of the double layer as its critical drawback. In the present study, we chose the PVP/P(VDF/TrFE) double layer for the top-gate insulator of our FeFETs. Since the leakage current paths of PVP and P(VDF/TrFE) films are different from each other, it is likely that our double-layered films should have a much improved dielectric strength.[10]

Figures 2(a) and 2(b) display the drain current-drain voltage (I_D-V_D) output and drain current-gate voltage (I_D-V_G) transfer characteristics obtained from the FeFET with PVP/P(VDF/TrFE) double layer in the pristine state, respectively. The output curves showed a typical field effect behavior but the I_D of our FeFET hardly saturates [Fig. 2(a)]. To investigate the electrical properties of our FeFETs in the pristine state, the gate voltage sweep was performed at a V_D of 10 V and at a scan rate of 5 V/s within the V_G range of ±40 V, which is less than the coercive voltage [51 V for our PVP/P(VDF/TrFE) double layer]. Maximum drain current of ~14 μA was achieved under a gate bias of 40 V. The on/off current ratio and the linear field effect mobility were determined to be 10^4 and 0.36 $cm^2/V\,s$, respectively, from the transfer curve [Fig. 2(b)]. No sign of I_D-V_G hysteresis was observed, yet and maximum gate leakage current was ~100 pA. While usual ZnO-based TFTs were reported to have a positive threshold voltage,[11,12] our FeFETs seem to show an early turn on with a negative threshold voltage. The reason is not clear but is probably due to process-involved positive fixed charges at the PVP-P(VDF/TrFE) interface. This speculation is quite acceptable because within the ±40 V scan range our device showed no I_D-V_G hysteresis, which means that no charge injection from gate electrode occurred during the sweep.[13,14] In contrast to our FeFET with the double-layer dielectric showing typical field effect be-

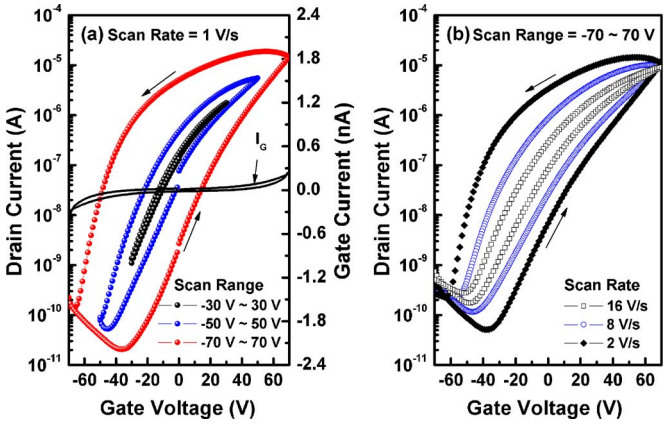

FIG. 3. (Color online) I_D-V_G transfer characteristics of our FeFETs with (a) various scan ranges (V_G=±30–±70 V) and with (b) various scan rates (2–16 V/s). I_G-V_G curve for the gate leakage level of our FeFET.

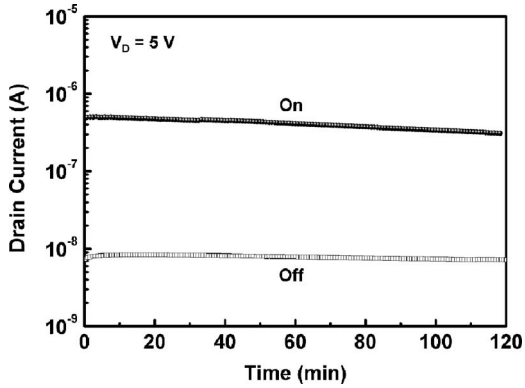

FIG. 4. Data retention properties of the on and off states of the FeFET under a floating gate (V_G=0 V, V_D=5 V) condition.

havior, the device with single P(VDF/TrFE) layer displayed no field effect but large amount of gate leakage (approximately equal to a few microamperes), as shown in Fig. 2(c) (Displacement current peaks were not observed here, either, probably due to the large current leakage.)

Figures 3(a) and 3(b) show the transfer characteristics for FeFET with our PVP/P(VDF/TrFE) double layer. Transfer characteristics in Fig. 3(a) were measured under V_D =10 V at a scan rate of 1 V/s with various scan ranges: ±30, ±50, and ±70 V. Our device showed negligible hysteresis with the ±30 V scan but displayed obvious counterclockwise hysteresis with the ±50 V scan which is close to the measured coercive voltage of our gate insulator (51 V). The hysteresis was enlarged by increasing the scan range and a very large hysteresis (the outermost loop) was achieved with the ±70 V scan surpassing ±51 V. According to the outermost loop in the transfer characteristics, the remnant current modulation of $\sim 3 \times 10^3$ was achieved at zero gate voltage. In view of the hysteresis size and the direction in Fig. 3(a), the memory effects of our FeFET originate from the switching behavior of the dipoles in the double-layer insulator [including P(VDF/TrFE) layer]. The solid line represents the gate leakage current (I_G) of the FeFET and the gate leakage level was as low as ~0.2 nA at maximum. Similar hysteresis behavior was again observed by changing the rate of ±70 V scanning, as shown in Fig. 3(b). The adopted rates were 2, 8, and 16 V/s. The slowest scan displayed the largest hysteresis loop and it means that the switching speed of the remnant dipoles in our ferroelectric layer is not high enough to fully follow the high scan rate.

Figure 4 shows data retention properties of the on and off states of our FeFET as obtained by measuring the drain current under a floating gate (V_G=0) condition with a constant drain voltage of 5 V for about 2 h. The FeFET was biased at V_G=±70 V for 15 s so that the device completely turns on (at +70 V) and turns off (at −70 V). Then the time evolution measurement of the drain current was performed to observe the retention properties of our FeFET with the double-layer insulator. Only a slight reduction in the initial value of the drain current was observed and the on/off current ratio changed from 66 to 43 during the measuring time. Comparable retention properties were reported with organic semiconductor channel on a single P(VDF/TrFE) layer but the organic channel FeFET showed two orders of magnitude lower carrier mobility than that of our ZnO-based FeFET with double-layer ferroelectric insulator, also displaying inferior leakage current characteristics as well.[8] Switching time of our FeFET was rather inferior to the literature (approximately equal to millisecond)[15] and the reason is not clear. We suspect the slow polarization in the underlying 450-nm-thick PVP layer[16] that would influence the dipole switching speed of the P(VDF/TrFE) layer attached on the PVP.

In summary, we have fabricated top-gate ZnO-TFTs with PVP/P(VDF/TrFE) double gate insulators for nonvolatile memory device. The PVP/P(VDF/TrFE) double layer showed ferroelectric switching behavior without serious leakage current. Our FeFETs with the double-layered gate insulators demonstrated a high field effect mobility of 0.36 cm^2/V s, large memory hysteresis in the transfer curve, and decent data retention properties, which originate from ferroelectric polarization of the P(VDF/TrFE) layer.

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