Pentacene-Based Low-Leakage Memory Transistor with Dielectric/Electrolytic/Dielectric Polymer Layers

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We report on the pentacene memory thin-film transistors (TFTs) with a poly-4-vinylphenol (PVP)/poly(vinylidene fluoride/trifluoroethylene) [P(VDF/TrFE)]/PVP triple-layer gate insulator. The top PVP dielectric in the triple layer was intended to provide a smooth hydrophobic surface to ensure good crystalline growth of pentacene channel, while the bottom PVP was for leakage protection. The middle P(VDF/TrFE) layer, known as ferroelectric material, revealed an electrolytic or ion movement signature rather than ferroelectric in our sandwich form of organic insulator. Our TFTs showed remarkably reduced leakage current, good memory window (large threshold voltage shift under slow gate-bias swing), and good field-effect mobility (0.2 cm^2/V s). Retention time for the electrolytic memory effects was measured to be more than 10^4 s under a constant-read condition.
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Poly(vinylidene fluoride/trifluoroethylene) [P(VDF/TrFE)] co-polymer, as a promising organic ferroelectric, has attracted recent attention for nonvolatile memory applications on glass substrates because of its large remnant polarization over 7.5 μC/cm^2, short switching time (~1 ms), and ease of fabrication in thin-film form by the solution process at low temperatures.[1,2] Recent reports have shown that organic semiconductor-based thin-film transistors (TFTs) with ferroelectric P(VDF/TrFE) have some memory performances such as nondestructive readout and good retention,[3-5] although those ferroelectric TFTs still have several extrinsic problems to be solved, such as high operating voltage of more than 50 V, low mobility, and high leakage current. Moreover, as an intrinsic problem of the ferroelectric nonvolatile memory (NVM) field-effect transistor, a channel-induced depolarization field persistently remains even after gate bias has been removed, seriously reducing the retention period in off-state (erase-state).[6] In the present work, we have fabricated pentacene-based NVM-TFT with organic triple-layer insulators of dielectric/ferroelectric/dielectric, inserting a P(VDF/TrFE) layer between the poly-4-vinylphenol (PVP) layers to solve the above-mentioned problems as well as to maintain decent NVM effects. As a result, we found an interesting NVM effect, not based on ferroelectric but rather on electrolytic behavior of the inserted P(VDF/TrFE) layer, with which our pentacene-TFT showed good field mobility and decent retention time without serious gate leakage but required long pulse periods for program (write) and erase.

Experimental

A 45 nm thick PVP film on a cleaned indium-tin-oxide (ITO, 30 Ω/□) glass was prepared from 2 wt % solutions of PVP by spin casting and subsequent curing at 175°C for 1 h in a vacuum oven. Then, 140 nm thick P(VDF/TrFE) ferroelectric film was spin-coated on the thin PVP using a 6 wt % solution of P(VDF/TrFE) 75/25 mol % copolymer and cyclohexanone, and then the film went through curing at 140°C for 2 h in air. After that, a 240 nm thick PVP overlayer was spin-coated on the P(VDF-TrFE) with 8 wt % solutions of PVP, followed by curing at 155°C for 1 h in a vacuum oven and subsequent in situ oven cooling. Pentacene channels were then patterned on our triple-layer insulator through a shadow mask at room temperature by thermal evaporation. The Au source/drain electrodes were finally deposited by thermal evaporation. The schematic cross-sectional view of Fig. 1a shows the triple-layer insulator and the channel with a nominal length (L) of 90 μm. The width/length (W/L) ratio of our TFTs was ~5.56. All electrical characterizations were carried out with a semiconductor parameter analyzer

(model HP 4155C, Agilent Technologies) and a capacitance meter (Mode HP 4284, 1 MHz) in the dark at room temperature. Displacement charge density-electric field (*D-E*) measurements [by using the same measurement technique as that for polarization-electric field (*P-E*) measurement] have also been carried out with the single P(VDF-TrFE) and the triple-layer insulator by using Sawyer–Tower circuits.[7] The thicknesses of the films were confirmed by a surface profiler (Alpha-Step IQ).

Results and Discussion

Figures 1b and c show the capacitance-electric field (*C-E*) and current density-electric field (*J-E*) characteristics of P(VDF/TrFE) single layer (140 nm thick) and our PVP/P(VDF/TrFE)/PVP triple layer as obtained from 300 μm diameter Al/insulator/ITO structures. The capacitance of the 140 nm thick P(VDF/TrFE) film varied from 43 to 63 nF/cm^2, so that the dielectric constant (k_{FE}) of the P(VDF/TrFE) film ranged from 6.7 to 9.9. The peaks of capacitance (Fig. 1b inset) and displacement current density (Fig. 1c inset) were observed at the same electric field, which must have shown the ferroelectric switching of the P(VDF/TrFE) film during voltage sweeps between −100 and 100 MV/m. From the peak positions of the *C-E* and *J-E* curves, the coercive field (E_c) of our P(VDF/TrFE) film was determined to be 50 MV/m. Based on the coercive field of P(VDF/TrFE) and the following equation,[8] the coercive voltage (V_c) for our 240 nm thick PVP/140 nm thick P(VDF/TrFE)/45 nm thick PVP triple layer was worked out to be ±43 V (102 MV/m)

$$V_c^{\text{triple-layer}} = E_c^{\text{FE}} \frac{k_{i1}k_{i2}t_{FE} + k_{i2}k_{FE}t_{i1} + k_{FE}k_{i1}t_{i2}}{k_{i1}k_{i2}} \quad [1]$$

where k_i, k_{i2}, and k_{FE} are the dielectric constants (~3.9)[9,10] of the two PVP and that (~9.9) of P(VDF/TrFE) films, respectively, and t_{i1}, t_{i2}, and t_{FE} are the respective thicknesses. Under an appropriate *E*-field range (or ±40 V) near coercive value, however, we could not observe any ferroelectric switching signature from our triple layer in the *C-E* and *J-E* measurements at all, while the triple layer resulted in 3 orders of magnitude lower leakage current density than that of the single P(VDF/TrFE) layer. The reason for losing ferroelectric signature is mainly attributed to the depolarization field[6] caused by the dielectric PVP layers sandwiching our ferroelectric layer. Instead, we found an interesting feature of the displacement-charge variation with *E*-field sweeping period from both the single- and triple-layer samples.

According to *D-E* measurements as shown in Fig. 2a, the displacement charge density (*D*) in the single P(VDF/TrFE) layer showed *E*-field dependent saturation under a fast sweeping rate of 11 V/s (7 MV/m s) and also showed its remnant value of
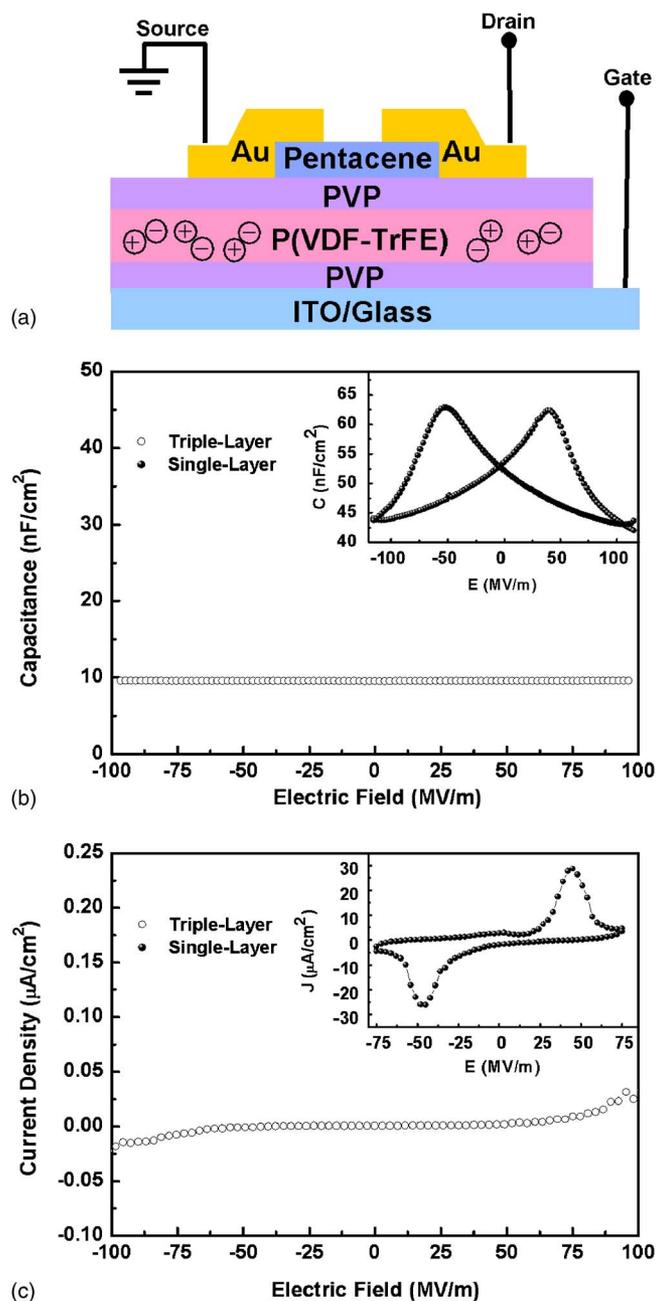
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Figure 1. (Color online) (a) Schematic cross section of our pentacene NVM-TFT with PVP/P(VDF/TrFE)/PVP. (b) Plots of *C-E*, characteristics of the P(VDF/TrFE) single layer (inset) and PVP/P(VDF/TrFE)/PVP triple layer. (c) *J-E* characteristics of the single (inset) and triple layers.

Figure 2. (Color online) (a) *D-E* measurements conducted with a single layer and (b) with a triple layer. Note that remnant-displacement charge density increases with the slow *E*-field sweep in both *D-E* measurements for single P(VDF/TrFE) and triple layers. The triple layer appears not to conserve any ferroelectric effects (polarization saturation) regardless of applying excessive *E*-field ($\sim$50 V) in sweeping.

$\sim$5.5 μC/cm^2, while the remnant D increases up to 8 μC/cm^2 under a much lower rate of 0.9 V/s (0.5 MV/m s). According to Fig. 2b, unlike the case of the single layer, our triple layer did not show any charge-saturation behavior under fast sweeping even when a higher E-field than coercive one was applied. However, under a slow E-field sweep the D-E curve appeared saturated and the remnant D value in our triple layer became as large as 2 μC/cm^2, although it was only $\sim$0.1 μC/cm^2 under the fast rate (Fig. 2b). These D-E results of Fig. 2a and b mean that our triple layer does not possess any ferroelectric properties, and moreover, the P(VDF/TrFE) component contains some electrolytic ions inside, so that those ions slowly move toward the PVP/P(VDF/TrFE) interfaces under the long-term E-field sweep, resulting in a considerable
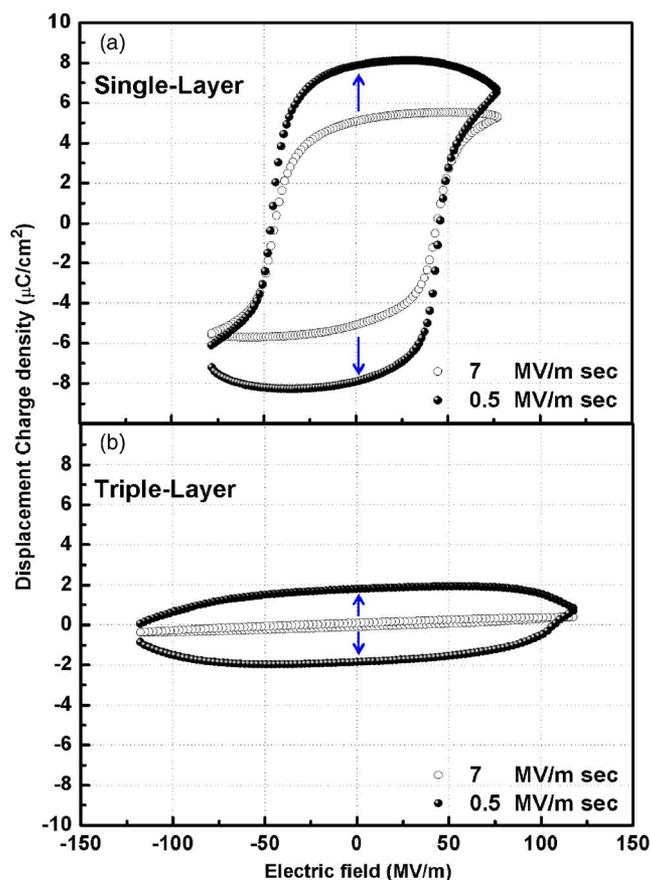
density-of-displacement charge [see the arrows indicating more than $\sim$2 μC/cm^2, which is in fact about the same magnitude of D increase as in the single P(VDF/TrFE) component (Fig. 2a)].

Figures 3a and b exhibit atomic force microscopy (AFM) images of pentacene films deposited on PVP and P(VDF/TrFE), respectively. Figure 3a shows the surface of typical crystalline pentacene with large dendritic grains,[10] promising a high field-effect mobility of our pentacene channel as deposited on PVP, the top element of the triple-layer dielectric. According to Fig. 3b, however, such good crystalinity of the pentacene channel could not be achieved on P(VDF/TrFE),[5] the intermediate element of the triple layer. Small-sized grains of pentacene were only observed after they are grown on the P(VDF/TrFE). Figures 3c and d show the AFM surface images of the top PVP and intermediate P(VDF/TrFE) layers, respectively. The root-mean-square (rms) surface roughness of 140 nm thick P(VDF/TrFE) film as $\sim$3.28 nm, while the 240 nm PVP overlayer improves the rms value to 0.7 nm. Therefore, the PVP overlayer is indispensable for achieving a good crystalline pentacene for high channel mobility and reducing gate-leakage current as well.

Our NVM-TFT with a PVP/P(VDF/TrFE)/PVP triple layer displayed a good hysteresis memory window as shown in the drain current-gate voltage (I_D-V_G) characteristics of Fig. 4a. [We also fabricated a reference TFT with only a P(VDF/TrFE) layer, but its device performance was too inferior to present here: a low mobility of 10^{-4} cm^2/V s and high gate leakage of a few μA.] The memory hysteresis of our NVM-TFT with a triple layer was only observed by adopting a high voltage range ($V_G = \pm$50 V) and a slow sweeping
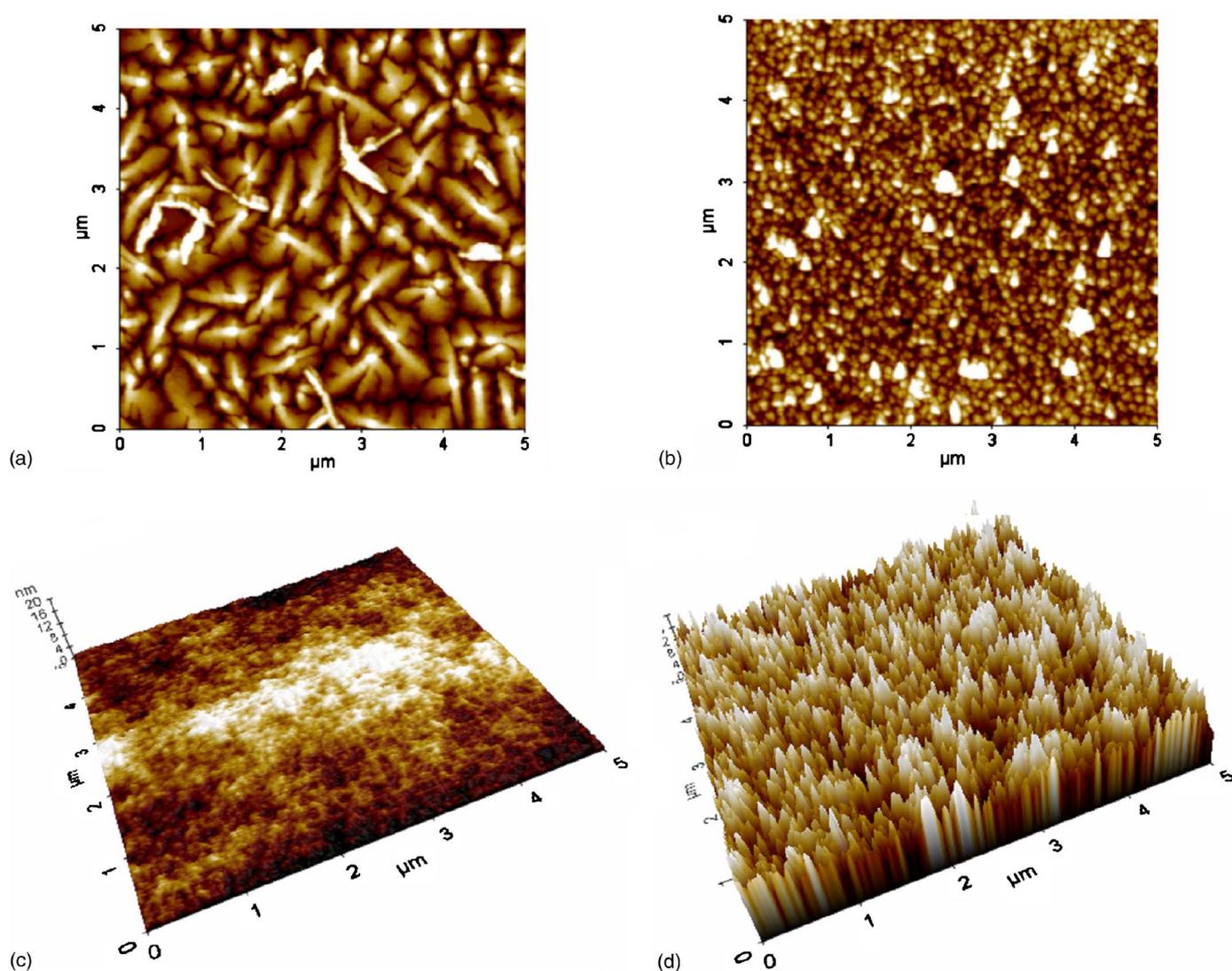
Figure 3. (Color online) AFM images of (a) pentacene films grown on PVP/P(VDF/TrFE)/PVP and (b) on P(VDF/TrFE)/PVP. (c) AFM surface images of PVP/P(VDF/TrFE)/PVP and (d) P(VDF/TrFE)/PVP.

rate (0.9 V/s), while no hysteresis was shown in a small sweeping range of -20 to 10 V under the same rate. In the present study, however, we could observe the memory effects within the small voltage range (-20 to 10 V) by initially pulsing our device with -50 V gate bias for 10 s (write, program) and then with $+50$ V for the same period (erase). Figure 4b displays the $\sqrt{I_D}$-V_G curves of our pristine TFT and those of gate-pulsed devices (both write and erase) as obtained by gate hysteresis sweep from -20 to 10 V. As estimated from Fig. 4b, the typical field-effect mobility (μ_{FET}) was 0.2 cm^2/V s, which is quite high for organic NVM-TFTs. According to our $\sqrt{I_D}$-V_G curves, the threshold voltage (V_{Th}) of the pristine device was -8 V, but it shifted to $+5$ V ($\Delta V_{Th} \approx 13$ V) after write pulse, while the V_{Th} shifted to -15 V ($\Delta V_{Th} \approx -7$ V) for erase. The values of V_{Th} shift were reversibly sustained even under 10 times of repeated gate-voltage sweeps (between -20 and 10 V), so that the I_D-V_G curve trace was almost precisely overlapped on the full-scale memory characteristics in Fig. 4a. Such write and erase (memory) effects were simply re-examined from the I_D-V_D output curves of pristine, write-pulsed, and erase-pulsed devices, as displayed in Fig. 4c. Our pentacene-based NVM-TFT shows a maximum saturation current of ~ 6.5 μA (at $V_G = V_D = -20$ V) in the write state (after -50 V pulse on gate), while the maximum I_D current of the pristine

was ~ 1.5 μA. However, the same device showed less than 0.4 μA after an erasing pulse of $+50$ V. Figure 4d shows data-retention properties of our NVM-TFT, which were regarded here as duration periods for the write- and erase-state I_D under zero gate bias ($V_G = 0$) conditions with a constant drain voltage (V_D) of -1 V. The pristine TFT was biased at $V_G = \pm 50$ V for 10 s prior to the measurement of the time evolution of the I_D for write and erase state. The write/erase state current ratio changed from 100 to 30 within 10^4 s (~ 3 h). The gradual loss of retention must be due to the slow ion movement inside the intermediate P(VDF/TrFE) layer under $V_D = -1$ V. Although we do not clearly know the identities of electrolytic ions inside, it is regarded that these electrolytic or ionic memory effects may provide useful device applications such as pulse-induced V_{Th} modification for coupled organic inverter.

Conclusion

In summary, we have fabricated pentacene NVM-TFTs with PVP/P(VDF/TrFE)/PVP triple-gate insulators on ITO/glass substrate. Our memory TFT with the triple layer showed a high mobility of 0.2 cm^2/V s along with much lower leakage current density than that of single P(VDF/TrFE). Due to a depolarization field, our
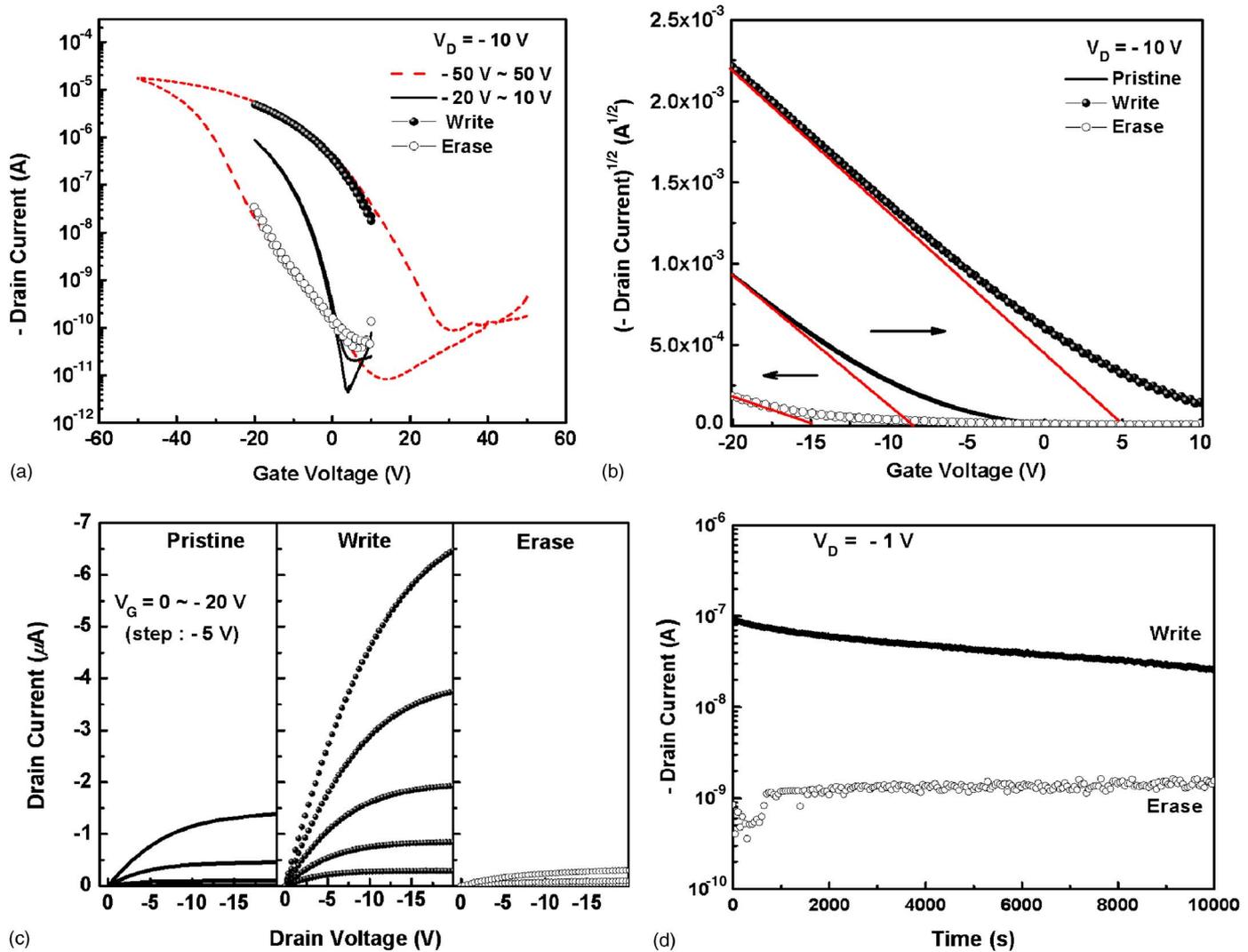
Figure 4. (Color online) (a) Transfer characteristics ($\mathrm{Log}_{10}I_D$-V_G) for memory hysteresis (dashed red) of our device as obtained by V_G sweeping from -50 to $+50$ V. Simple transfer curves obtained between -20 and 10 V do not show any hysteresis features, but after write (-50 V pulsed) and erase ($+50$ V pulsed), those curves trace the memory-effect tracks of I_D. (b) $\sqrt{I_D}$-V_G curves obtained between -20 and 10 V after ±50 V 10 s gate pulsing. Large V_{Th} shifts are observed from $\sqrt{I_D}$-V_G, curves, 13 V for write and -7 V for erase. Our pristine device exhibited a high mobility of ~ 0.2 cm^2/V s. (c) The three output (I_D-V_D) curves of our device. (d) Data retention properties of the write and erase states of our NVM-TFT as measured under zero gate ($V_G = 0$ V) condition and constant drain voltage ($V_D = -1$ V).

NVM-TFT did not show any ferroelectric memory effects but displayed a good electrolytic memory window and large V_{Th} shift that are obtained by ion movement under long-term pulse (10 s). We thus believe that decent retention and good V_{Th} modification properties of our device can provide some promising and specific future applications.

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