Journal of The Electrochemical Society, **154** (11) H933-H938 (2007)
0013-4651/2007/154(11)/H933/6/$20.00 © The Electrochemical Society

Systematic Studies on Low-Voltage Pentacene Thin-Film Transistors with Low-*k* Polymer/High-*k* Oxide Bilayer Gate Dielectric

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We report on the fabrication and characterization of pentacene based thin-film transistors (TFTs) with low-*k* poly-4-vinylphenol (PVP)/high-*k* yttrium oxide (YO_x) bilayer gate dielectrics of various thickness combinations, for the thin-PVP layers (45, 70, and 140 nm) and for the thin YO_x (50 and 100 nm). Neither YO_x nor thin-PVP single layer film alone can properly function as a dielectric layer due to their very high leakage current. However, our bilayer films of six different thickness combinations (among which the thinnest was PVP/YO_x = 45/50 nm while the thickest was PVP/YO_x = 140/100 nm) all exhibited quite a good dielectric strength of ~2 MV/cm, based on our maximum leakage current standard of 10^{-6} A/cm^2. All pentacene TFTs with the PVP/YO_x bilayer gate dielectric films successfully demonstrated good TFT characteristics at an operating voltage less than −5 V. In particular, two of our devices studied here with the bilayer combinations (45 nm thin PVP on 50 nm and 100 nm thick YO_x) exhibited good device performance with field effect mobilities (1.74 and 1.05 cm^2/V s) and an on/off current ratio of ~10^4. We also demonstrate a resistance-load inverter operating below −5 V with a load resistance (R_L) of 22 MΩ connected to our pentacene TFT with a PVP (45 nm)/YO_x (100 nm) layer.
 [DOI: 10.1149/1.2775169]

Manuscript submitted December 4, 2006; revised manuscript received July 2, 2007. Available electronically September 4, 2007.

Organic electronics has been a subject of active research over the last few decades. In particular, organic thin-film transistors (OTFTs) have been extensively investigated due to their potentials for practical applications: drivers for flat-panel displays, low-end smart cards, and radio-frequency identification tags.[1-4] Conventional OTFTs need more than 15 V for gating and charge-transport operations to achieve device characteristics. However, for portable and battery-powered applications requiring low power consumption, it is essential to reduce the operating voltage to below 5 V.[5,6]

For low voltage operation, there are two general approaches to obtain a high capacitance of gate dielectrics: by increasing the dielectric constant or by reducing the dielectric thickness. Since Dimitrakopoulos et al. reported low-voltage-driven OTFTs with high-*k* dielectric layers,[7] many research groups have fabricated low-voltage-driven OTFTs adopting high-*k* metal oxides (Ta_2O_3, TiO_2, etc.).[8-11] However, conventional high-*k* inorganic gate dielectric films are generally thick (typically, more than ~100 nm) in the interest to avoid serious gate leakage current. These oxides are not quite suitable for direct growth of an organic semiconductor channel due to their highly hydrophilic surfaces. Such surfaces are likely to cause undesirable interface interactions with organic semiconductors and cause device instability such as gate voltage hysteresis.[11] On the other hand, another types of low-voltage-driven OTFTs adopting ultrathin gate dielectrics such as self-assembled-monolayer[12,13] and thin polymers[14-16] have also been reported. Ultrathin organic gate dielectrics readily accommodate an organic semiconductor channel but are still problematic due to their structural imperfections including pinholes generated during the deposition processes.[9,14,15] One way to circumvent the aforementioned drawbacks from inorganic high-*k* and ultrathin organic dielectrics is to stack an organic layer on a high-*k* inorganic film, hence selectively combining the advantages of both gate materials. In previous studies, we thus have reported on the fabrication and characterization of thin-film transistors (TFTs) with poly-4-vinylphenol (PVP)/high-*k* yttrium oxide (YO_x) or PVP/rf-sputter-deposited AlO_x bilayer gate dielectrics and demonstrated organic TFTs with a 45 nm PVP/100 nm high-*k* oxide combination operating at low voltages under 5–8 V.[17,18] In this paper, we extend systematically these experiments to wider thickness ranges of polymer/high-*k* oxide combinations for pentacene TFTs. These experiments are systematically investigated in the present article, where we fabricated pentacene TFTs with PVP/YO_x gate dielectrics of various thickness combinations (PVP/YO_x = 45 nm/50 nm, 70 nm/50 nm, 140 nm/50 m, 45 nm/100 nm, 70 nm/100 nm, and 140 nm/100 nm) and studied in detail the resulting device performance characteristics (see Tables I and II).

Experimental

Prior to the deposition of dielectric films on indium-tin oxide (ITO) glass, the glass was cleaned with acetone, ethanol, and deionized water in that order. The thickness and sheet resistance of the ITO films were 79 nm and 30 Ω/□. Subsequently, yttrium oxide (YO_x) films were deposited by electron-beam evaporation using 99.999% Y_2O_3 pellets in a vacuum chamber at room temperature (RT) [the initial base pressure was about 5×10^{-7} Torr and the working pressure of O_2 gas was fixed at 1×10^{-4} Torr]. The thickness of YO_x film was set to 50 and 100 nm as monitored by a quartz crystal oscillator and the value was confirmed by a surface profiler (Alpha-Step IQ). PVP films were then prepared from solutions of PVP and poly(melamine-*co*-formaldehyde), as a cross-linking agent, in propylene glycol monomethyl ether acetate, by spin coating and subsequent cross-linking (curing) at 175°C for 1 h in a vacuum oven. The final thicknesses of the PVP films were approximately 45, 70, and 140 nm as measured by the surface profiler. Pentacene (Aldrich Chem. Co., ~99% purity) channels were patterned on the PVP/YO_x layers through a shadow mask at a substrate temperature of RT by thermal evaporation. We fixed the deposition rate to 1 Å/s using an effusion cell (Alphaplus Co., LTE-500S) in a vacuum chamber (base pressure ~1×10^{-7} Torr). The thickness of the pentacene film was 50 nm as monitored by a quartz crystal oscillator and confirmed by ellipsometry. The source/drain (S/D) Au electrodes were finally deposited by thermal evaporation. As shown in the schematic cross-sectional view of the Fig. 2 inset, the nominal channel length (L) and width (W) of our pentacene TFTs were 90 and 500 μm, respectively.

The compositions (stoichiometry) of the oxide films were measured by 2 MeV $^4He^{2+}$ Rutherford backscattering spectrometry (RBS) using the sample deposited on p-Si substrates. X-ray diffraction (XRD) measurements were performed with monochromatic Cu Kα (λ = 1.54 Å) radiation to investigate the crystalline qualities of YO_x films and those of the pentacene films deposited on YO_x and PVP layers. The surface of each layer was characterized by atomic force microscopy (AFM) [Nanoscope IV, Digital Instruments]. The electrical properties of the PVP/YO_x sandwiched gate dielectric

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Table I. Electrical and surface properties of single YO_x, single PVP films, and PVP/YO_x bilayers.

Dielectric	Thickness (nm)	Dielectric strength (MV/cm)	Capacitance (nF/cm^2)	Surface roughness (nm)
YO_x	50	···	258 (estimated)	2.15
YO_x	100	0.2	129	1.83
PVP	45	···	76.7(estimated)	0.46
PVP	70	0.1	47.3	0.4
PVP	140	0.1	26.0	0.32
YO_x/PVP (Type 1)	45/50	2	70.8	1.06
YO_x/PVP (Type 2)	70/50	2	44.3	0.73
YO_x/PVP (Type 3)	140/50	2	24.3	0.66
YO_x/PVP (Type 4)	45/100	2	47.1	0.78
YO_x/PVP (Type 5)	70/100	2	35.2	0.62
YO_x/PVP (Type 6)	140/100	2	21.9	0.48

films were measured with Au/dielectric/ITO glass structures through capacitance-voltage (*C-V*) and current density-electric field (*J-E*) tests. All current-voltage (*I-V*) characteristics of our TFTs, test structures, and resistance-load inverters were measured with a semiconductor parameter analyzer (HP 4155C, Agilent Technologies). The *C-V* measurements were made with a HP 4284 capacitance meter (1 MHz) in the dark at RT. The dynamic response of our resistance-load inverter was measured with a function generator (AFG310, Sony/Tektronix) and an oscilloscope (TDS210, Tektronix).

Results and Discussion

Figures 1a and b exhibit the typical RBS spectra of our 50 and 100 nm thick YO_x films on p-Si. As simulated by the RUMP code, the stoichiometry of our oxide films was identified to be close to YO_3. Our oxide films were amorphous, as observed in the XRD spectra of Fig. 2. The composition of our oxide films deviated from the ideal bulk stoichiometry and those oxides tend to be amorphous due to room temperature processing.[19-21] Generally, oxide films are deposited or postannealed in an oxygen ambient to avoid an easy oxide–breakdown.[19,20] Our YO_x films were also deposited in oxygen ambient and thus an oxygen-rich stoichiometry was observed. It is inferred that nonbonding oxygen atoms probably exist inside our amorphous YO_x films and, according to the literature,[19-22] stoichiometric crystalline Y_2O_3 films might be obtained when the oxide films were annealed at an elevated temperature higher than 450°C, which is unfortunately not compatible with the fabrication of OTFT.

Figures 3a and b display the *J-E* and *C-V* characteristics resulting from Au/insulator/ITO structures with single thick PVP (140 nm), single thick YO_x (100 nm), the thinnest PVP/YO_x (45 nm/50 nm), and the thickest bilayer (140 nm/100 nm) combinations (the dielectric strength and capacitance values of all our single and bilayer films are summarized in Table I). The bare YO_x and PVP films turned out to be inadequate as a dielectric layer, since they exhibited very high leakage current. However, all PVP/YO_x bilayers showed quite a good dielectric strength of ~2 MV/cm based on our maximum leakage current standard of $\sim 10^{-6}$ A/cm^2, as shown in Table I and Fig. 3a. It is interesting to note that although the total thickness of the thinnest bilayer (45/50 nm) is only 95 nm, its dielectric strength is superior to those of 100 nm thick YO_x and 140 nm thick PVP single layers. We thus regard that the leakage current paths of YO_x and PVP films are different from each other and are not connected, so that our organic-inorganic bilayers possess a much improved dielectric strength.

The capacitances of the PVP (45 nm) and YO_x (50 nm) single layers could not be measured (but just estimated) because of their high leakage current but those of 70 , 140 nm thick PVP and 100 nm thick YO_x single layer films were successfully measured, to be about 47.3, 26.0, and 129 nF/cm^2, respectively (Table I). According to Table I, the dielectric constant, k, of the YO_x and PVP films was estimated to be ~14.6 and ~3.9, respectively. The stoichiometric crystalline Y_2O_3 film was reported to have k values of 17–20,[19,20,22] comparable to our YO_x film with a value of k (=14.6) in spite of its off stoichiometry as observed in its RBS results. The k of PVP was also similar to the previously reported values.[23,24] The thinnest bilayer of PVP (45 nm)/YO_x (50 nm) exhibited quite a high capacitance value (70.8 nF/cm^2). Based on the Eq. 1, the theoretical capacitance value of bilayer films can be estimated

$$\frac{1}{C_{\text{total}}} = \frac{1}{C_{\text{PVP}}} + \frac{1}{C_{\text{YO}_x}} \qquad [1]$$

The theoretical capacitance value of the thinnest PVP (45 nm)/YO_x (50 nm) layer is calculated to be ~60 nF/cm^2, taking the experimental k values of single PVP and YO_x, which results in a

Table II. Performance parameters of our pentacene TFTs with PVP/YO_x bilayer gate dielectrics of different thickness combinations.

Dielectric	Mobility ($cm^2/V\ s$)	Threshold voltage (V)	On/off current ration	Subthreshold swing (V/dec)
Type 1	1.74	−2.5	2×10^4	0.6
Type 2	0.96	−2.5	9×10^3	0.6
Type 3	0.30	−2.5	6×10^3	0.6
Type 4	1.05	−2.5	10^4	0.55
Type 5	0.67	−2.5	4×10^3	0.6
Type 6	0.20	−2.5	3×10^3	0.8

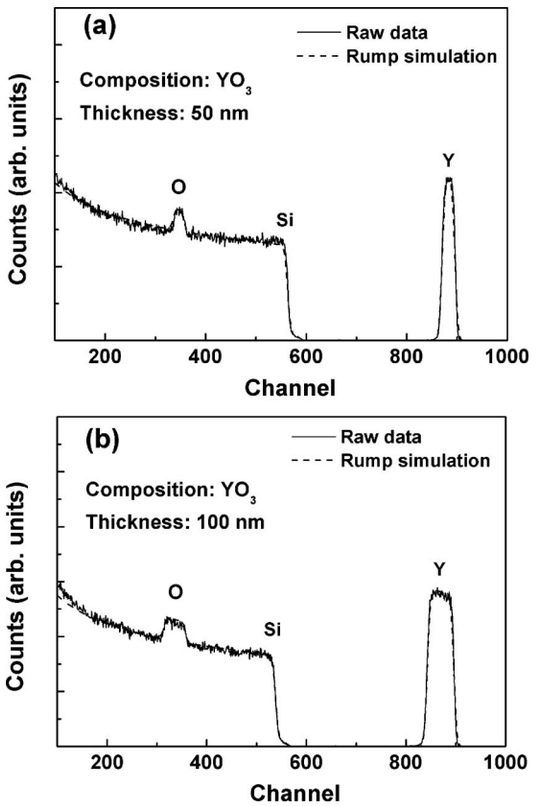

Figure 1. RBS spectra of yttrium oxide films of (a) 50 nm and (b) 100 nm deposited on p-Si substrates, and also RUMP simulation was performed to extract the stoichiometry of oxide.

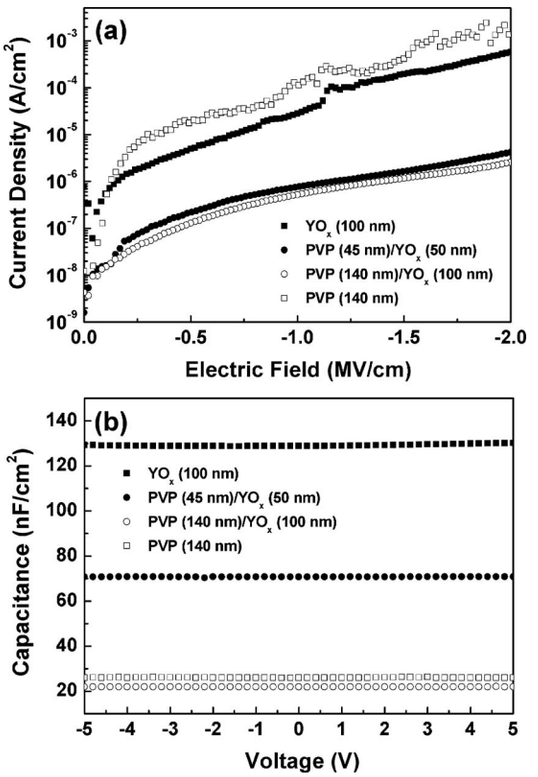

Figure 3. Plots of (a) *C-V* and (b) *J-E* characteristics measured with Au-dot/dielectric insulator/ITO structures. Chosen dielectrics were YO_x (100 nm), PVP (140 nm), the thinnest PVP/YO_x (45 nm/50 nm), and the thickest PVP/YO_x (140 nm/100 nm) combinations.

somewhat lower value than that of our experimental value (70.8 nF/cm^2). However, most of the other bilayer combinations showed little difference between the measured and theoretical values based on a model employing serially connected capacitors.

Figures 4a-d show the AFM surface images of 50 nm, 100 nm thick YO_x films and 45 nm thick PVP films deposited on those two YO_x films. The root-mean-square (rms) surface roughness values of all single and bilayers on ITO glass are summarized in Table I. The surface roughness of 50 nm and 100 nm thick YO_x films on ITO glass was 2.15 and 1.83 nm as shown in Fig. 4a and b, which improved to 1.06 and 0.78 nm, respectively (Fig. 4c and d) when 45 nm thick PVP dielectric films were deposited by spin coating. It is because viscose PVP solutions must have filled up the valley regions on the YO_x surface during the spin coating. According to Table I, the bilayer surface tends to be smoother with the thicker layer of PVP.

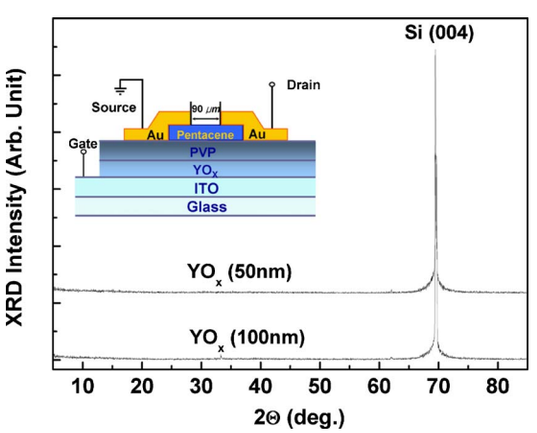

Figure 2. (Color online) XRD spectra obtained from YO_x films of (a) 50 nm and (b) 100 nm deposited on p-Si substrates. The XRD spectra show that all the oxide films are amorphous phase. The inset is a schematic cross-sectional view of our pentacene-based TFTs (channel length, L = 90 μm, width, W = 500 μm).

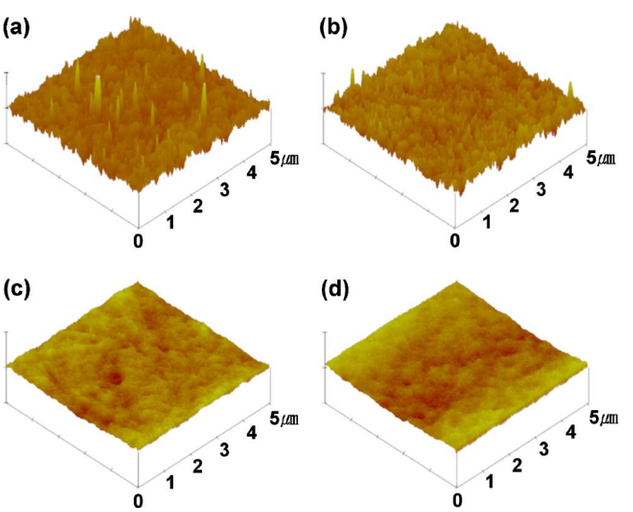

Figure 4. (Color online) AFM images obtained from dielectrics; (a) 50 nm thick YO_x, (b) 100 nm thick YO_x, (c) PVP (45 nm)/YO_x (50 nm), and (d) PVP (45 nm)/YO_x (100 nm) layers.

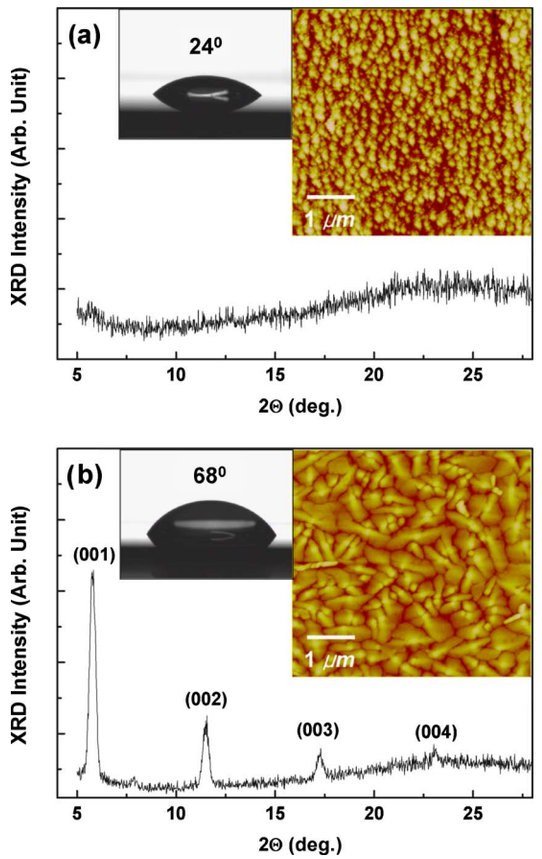

Figure 5. (Color online) XRD spectra and AFM images obtained from pentacene films deposited on (a) the 100 nm thick YO_x single layer and (b) on the PVP (45 nm)/YO_x (100 nm) bilayer. The insets are the contact angle data measured on the surfaces of the bare YO_x and the PVP/YO_x bilayer. We used deionized water for the measurements.

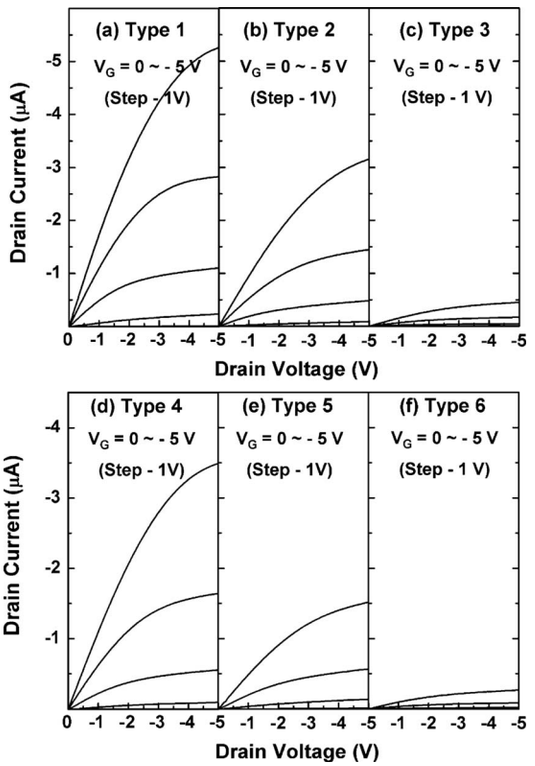

Figure 6. Drain current-drain voltage (I_D-V_D) output curves obtained from (a) type 1, (b) type 2, (c) type 3, (d) type 4, (e) type 5, and (f) type 6 devices.

The smoothened surface is important in that it becomes the channel/dielectric interface after pentacene growth. Rough interfaces or rough channels degrade the hole mobility. In this context, our PVP overlayer approach is considered quite effective.

The XRD spectra in Fig. 5a and b show that the crystallinity of active pentacene channels is influenced by the surface conditions of the substrate materials. While the pentacene film deposited on the YO_x layer exhibited no reflection peaks (which indicates that its phase is almost amorphous), the film grown on the PVP layer showed a good crystalline quality as judged by the number and intensity of resolvable diffraction peaks. Generally, the growth of the pentacene channel layer is strongly affected by the dielectric surface conditions such as its roughness and chemical state.[25-28] In addition to improving the rms roughness of dielectric surfaces (shown in Fig. 4a-d), our PVP layers have changed the chemical state (surface energy) of dielectric surface from hydrophilic to more hydrophobic, as experimentally proven in the contact angle measurements (see Fig. 5a and b insets). The contact angle measured on the bare YO_x film was only about 24° while it increased to 68° on the PVP film on YO_x. The nicely cured PVP layer forms a less-interacting interface with the pentacene channel while inorganic dielectrics make some undesirable interface interactions with the organic channel layer.[11,28] As a result, the pentacene grown on the smooth hydrophobic PVP/YO_x bilayer exhibited a good crystalline phase while the other one grown on the rough hydrophilic YO_x layer appeared amorphous. AFM images also support the XRD results. As expected, the pentacene film on the bare YO_x layer shows very poor surface morphology but it exhibits well-formed dendritic grains on the PVP-coated YO_x layer. Based on the aforementioned AFM, XRD, *J-E*, and *C-V* results, we believe that our scheme of fabricating a pentacene TFT with the PVP on top of the YO_x could be an effective approach to achieve a high-quality pentacene channel and quite a good dielectric capacitance as well.

Figures 6a-f show the drain current-drain voltage curves (I_D-V_D) obtained from our pentacene-based TFTs with six types PVP/YO_x bilayers of different thickness combinations: type 1 (PVP/YO_x = 45/50 nm), type 2 (PVP/YO_x = 70/50 nm), type 3 (PVP/YO_x = 140/50 nm), type 4 (PVP/YO_x = 45/100 nm), type 5 (PVP/YO_x = 70/100 nm), and type 6 (PVP/YO_x = 140/100 nm). All types of devices successfully demonstrated desirable TFT characteristics at an operating voltage lower than −5 V although type 3 and type 6 TFTs show a relatively low drain current less than ~1 μA. Maximum saturation current of ~5.2 μA was achieved under a gate bias (V_G) of −5 V from the type 1 device (the thinnest bilayer combination). With the increase of the total dielectric thickness, maximum saturation currentdecreased because the gate capacitance decreases.

Performance parameters, such as mobility, threshold voltage, on/off current ratio, and subthreshold swing, were determined from the $\sqrt{-I_D}$ vs V_G and $-I_D$ vs V_G curves of Fig. 7a and b. Such parameters for all our devices are summarized in Table II. According to the saturation-mobility estimation based on the $\sqrt{-I_D}$ vs V_G slope of the curves, the type 1 device with the thinnest bilayer exhibits the highest mobility of 1.74 cm^2/V s among all devices studied here although the other types of devices still have satisfactory mobilities as shown in Table II. In particular, the type 2 and type 4 devices exhibited quite good field effect mobilities of 0.96 and 1.05 cm^2/V s. It is clearly noted that the field effect mobility proportionally increases with the total dielectric capacitance of the bilayer. When dielectric capacitance increases, the mobility also tends to increase[7,29] because a higher capacitance would cause a higher hole density at the channel/dielectric interface where the accumulated

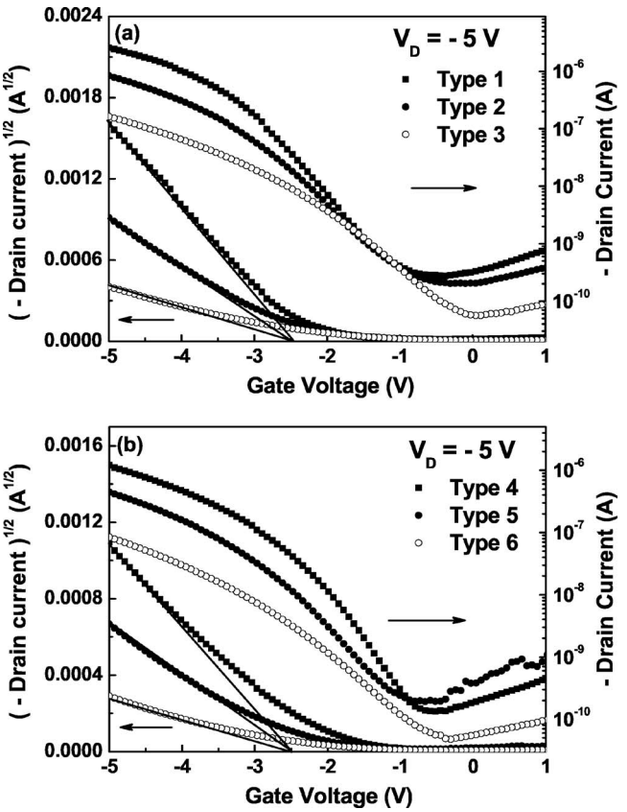

Figure 7. $\sqrt{-I_D} - V_G$ and $\mathrm{Log}_{10}(-I_D) - V_G$ plots obtained from (a) type 1, 2, 3 and (b) type 4, 5, 6 devices under a drain saturation condition ($V_D = -5$ V).

holes are used up to initially fill deep traps and then are transported to the drain. As a result, the higher capacitance in thinner dielectric bilayer would lead the TFT to have an enhanced mobility with higher drain current. The dielectric capacitance of an OTFT is thus very important, since it resultantly influences the drain current and field mobility of the device if the other conditions such as channel crystallinity,[25,26,28,30] channel/dielectric interface roughness,[25,26,28,31] and channel/electrode S/D contact[32] are identically controlled. Threshold voltages for all types of devices appeared similar to be about −2.5 V. According to the plots of $\log_{10}(-I_D) - V_G$ of Fig. 7a and b, the on/off current ratios for all devices were estimated to range from 3×10^3 to 2×10^4 and their subthreshold slopes were in the range of 0.55–0.8 V/dec. The performance of our devices is comparable to or better than previously reported cases.[7-16]

Anticipating low voltage operation, we set up a resistance-load inverter consisting of a pentacene TFT (type 2 device) and a load resistor (discrete load resistance, $R_L = 22$ MΩ) (see the inset of Fig. 8a for the inverter scheme). Our inverter operated well below 5 V showing a clear inverting response (input-to-output switching) between −5 V ("high") and 0 V ("low"). The inverter exhibits an output voltage hysteresis of ~0.5 V, which is mainly attributed to dielectric residual effect such as slow polarization due to −OH groups or gate charge injection, which may occur during gating.[24,33] The measured voltage gain, dV_{out}/dV_{in}, which is a parameter important to the subsequent stage switching, was ~3. The dynamic operation of this inverter was also demonstrated with our inverter setup. For the gate dynamics we adopted a dc pulsing for pulsed $V_{in} = -5$–0 V this time and used an oscilloscope with a buffer operational amplifier for sampling V_{out}. Figures 8b-d exhibit the dynamic behavior of our pentacene-based inverter, which was demon-

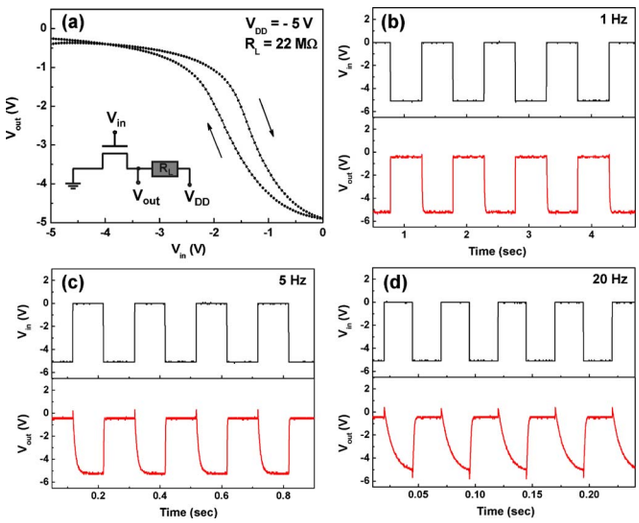

Figure 8. (Color online) (a) Static characteristics of our resistance-load inverter composed of a pentacene TFT with PVP (45 nm)/YO_x (100 nm) dielectric and a load resistor ($R_L = 22$ MΩ); inset shows a schematic circuit diagram of the inverter setup. Dynamic switching behavior demonstrated at various frequencies: (b) 1 Hz, (c) 5 Hz, and (d) 20 Hz. Upper pulse is the input (V_{in} pulse) driven by pulse generator and lower one is the measured output signal (V_{out}).

strated with various frequencies: 1, 5, and 20 Hz. At all frequencies the dynamic inverting was observed. At 20 Hz the spikes of V_{out} and *RC* delays at on-and-off switching appeared clear due to a large overlap capacitance between gate and S/D electrodes in our common gate structure. In particular, the rising time (t_r) at TFT-on state and falling time (t_f) at TFT-off state are significantly different, to be about 1.5 and 12 ms, respectively. It is because the channel resistance at the transistor-on state (~2 MΩ) was an order of magnitude lower than the load resistance at the TFT-off state (~22 MΩ). As a result, the RC delay at the turn-off state (the falling time) becomes much longer than at the turn-on state. The dynamic response could thus be enhanced by patterning the gate electrode (to reduce overlap capacitance).

Conclusion

We have fabricated pentacene-based TFTs and resistance-load inverters operating at a low voltage of −5 V, using PVP/YO_x bilayer gate dielectrics. Neither the YO_x nor PVP single layer dielectric alone can properly function as a dielectric layer due to their high leakage current. However, our bilayer films of six different thickness combinations (among which the thinnest combination was PVP/YO_x = 45/50 nm and the thickest was PVP/YO_x = 140/100 nm) exhibited quite a good dielectric strength of ~2 MV/cm and high capacitances (maximum ~70.8 nF/cm^2). The low-*k* PVP was found to complement efficiently the high-*k* oxide which has a rough hydrophilic surface, resulting in a smoothened hydrophobic surface, consequently allowing good crystalline pentacene channel growth on that surface. All the pentacene TFTs with the PVP/YO_x bilayer combinations as a gate dielectric successfully demonstrated desirable TFT characteristics operating at a voltage lower than −5 V. In particular, two types of devices with PVP (45 nm)/YO_x (50 and 100 nm) combinations exhibited excellent device performances with field effect mobilities (1.74 and 1.05 cm^2/V s, respectively) and on/off current ratios of ~10^4. A resistance-load inverter adopting our pentacene TFT with the PVP (45 nm)/YO_x (100 nm) layer and a load resistance (R_L) of 22 MΩ demonstrated good static/dynamic operations with a voltage gain of ~3 under 5 V. We thus conclude that our hybrid approach adopting

the low-k PVP/high-k YO_x bilayer as a gate dielectric is very effective in realizing a high performance low-voltage pentacene TFT, combining the merits of both materials.

Acknowledgments

The authors are very appreciative of the financial support from KOSEF (program no. 2002-03177), LG. Philips LCD, and they also acknowledge the support from Brain Korea 21 Project. J.H.K. acknowledges financial support from the Electron Spin Science Center at Postech, funded by KOSEF/MOST.

Yonsei University assisted in meeting the publication costs of this article.

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