Electrochemical and Solid-State Letters, **10** (4) H117-H119 (2007)
1099-0062/2007/10(4)/H117/3/$20.00 © The Electrochemical Society

Low-Voltage Pentacene Thin-Film Transistor with a Polymer/YO_x/Polymer Triple-Layer Dielectric on a Plastic Substrate

D. K. Hwang,[a] Jeong-M. Choi,[a] Ji Hoon Park,[b] Jae Hoon Kim,[a] Eugene Kim,[b] and Seongil Im[a,z]

[a]*Institute of Physics and Applied Physics, Yonsei University, Seoul 120-749, Korea*
[b]*Department of Information and Display, Hongik University, Seoul 121-791, Korea*

We report on the fabrication of pentacene thin-film transistors (TFTs) with a poly-4-vinylphenol (PVP)/yttrium oxide (YO_x)/PVP triple-layer dielectric deposited on an indium-tin oxide (ITO)/plastic substrate. Our PVP/YO_x/PVP triple layer exhibited 2 orders of magnitude lower gate current leakage than that of a PVP/YO_x double layer because the former has a PVP buffer to cope with the irregular surfaces of the ITO/plastic substrate. Adopting the triple-layer dielectric, our pentacene TFTs with NiO_x and Au source/drain electrodes exhibited high field mobilities of ~1.37 and 0.84 $cm^2/V\,s$, respectively, under low driving voltage conditions (less than −8 V). We conclude that our triple-layer approach is quite a promising and practical way to realize a flexible low-voltage high-performance organic TFT on ITO/plastic substrates with rough surfaces.
 [DOI: 10.1149/1.2432939]

Manuscript submitted September 12, 2006; revised manuscript received November 9, 2006.
Available electronically January 19, 2007.

Organic electronics has been a subject of active research over the last few decades. In particular, organic thin-film transistors (OTFTs) have been extensively investigated due to their potentials for practical applications: drivers for flat-panel displays, low-end smart cards, and radio-frequency identification (RFID) tags.[1-4] Conventional OTFTs need more than 15 V to be fully operational, which is incompatible with portable, battery-powered applications. Recently, low-voltage-driven OTFTs have been demonstrated by several research groups, adopting high-*k* oxide[5-7] or ultrathin organic gate dielectrics such as self-assembled monolayers (SAMs)[8,9] and thin polymers.[10-12] In our previous study, we used a hybrid polymer/high-*k* oxide double-layer dielectric to achieve a low-voltage OTFT fabricated on a glass substrate.[13] However, in order to fully utilize the key advantages of organic electronics, the hybrid dielectric system should be adapted to flexible nonfragile substrates, which usually have more irregular surfaces than those of glass substrates while the rough and irregular gate-substrate interface probably cause serious gate current leakage during device operation.[14,15]

In the present work, we have fabricated pentacene thin-film transistors (TFTs) with a poly-4-vinylphenol (PVP)/high-*k* yttrium oxide (YO_x)/PVP sandwich dielectric that is able to readily accommodate the rough surfaces of indium-tin oxide (ITO)/plastic substrate. Our pentacene TFTs fabricated on a plastic substrate have clearly demonstrated their low-voltage operation as a component of a resistance-load inverter (at less than −8 V).

Experimental

Prior to the deposition of dielectric films on an ITO-coated polyethylenenaphthalate (PEN) plastic substrate, the substrate was cleaned with methanol and deionized water, in that order. The first solid PVP film was prepared from solutions of PVP and poly(melamine-*co*-formaldehyde), as a cross-linking agent, in propylene glycol monomethyl ether acetate (PGMEA), by spin coating and subsequent cross-linking (curing) at 175°C for 1 h in a vacuum oven. The final thicknesses of the PVP films were approximately 45 nm as measured by a surface profiler (Alpha-Step IQ). YO_x films were then deposited on PVP by electron-beam evaporation using 99.999% Y_2O_3 pellets in a vacuum chamber at room temperature in O_2 ambient. The thickness of YO_x film was set to 50 nm and confirmed by the surface profiler. As the third layer, another 45 nm thick PVP film was spin-coated on YO_x/PVP layers. Pentacene (Aldrich Chem. Co., ~99% purity) channels were then patterned on our triple-sandwich dielectric layer through a shadow mask at room temperature by thermal evaporation. We fixed the deposition rate to 1 Å/s using an effusion cell (Alphaplus Co., LTE-500S) in a vacuum chamber (base pressure $\approx 1 \times 10^{-7}$ Torr). The pentacene film thickness was 50 nm as monitored by a quartz crystal oscillator and confirmed by ellipsometry. The source/drain (S/D) electrodes (NiO_x or Au) were finally deposited by thermal evaporation. The schematic cross-sectional view of Fig. 1a shows the triple-dielectric layer and the nominal channel length (L) of 90 μm. The width/length (W/L) ratio of our pentacene TFTs was ~5.56. The photograph in Fig. 1b displays our pentacene-based semitransparent TFT arrays (with NiO_x S/D electrodes) fabricated on a flexible PEN substrate.

The electrical properties of the gate-dielectric films were measured on Au/dielectric/ITO structures on PEN by capacitance–

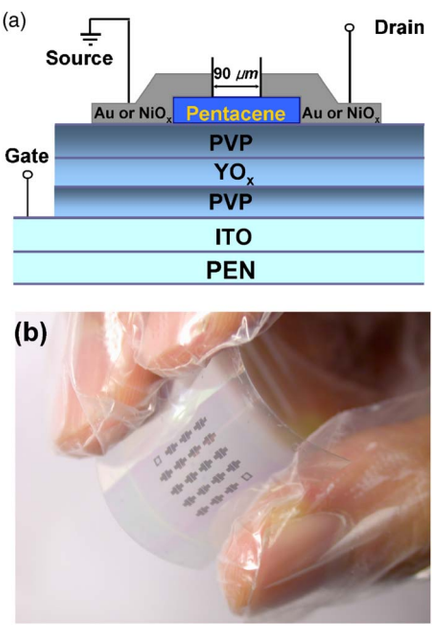

Figure 1. (Color online) (a) Schematic cross-sectional view of our pentacene-based TFTs (channel length, L = 90 μm, width, W = 500 μm) and (b) photographic view of our TFT array fabricated on a flexible PEN substrate.

[z] E-mail: semicon@yonsei.ac.kr

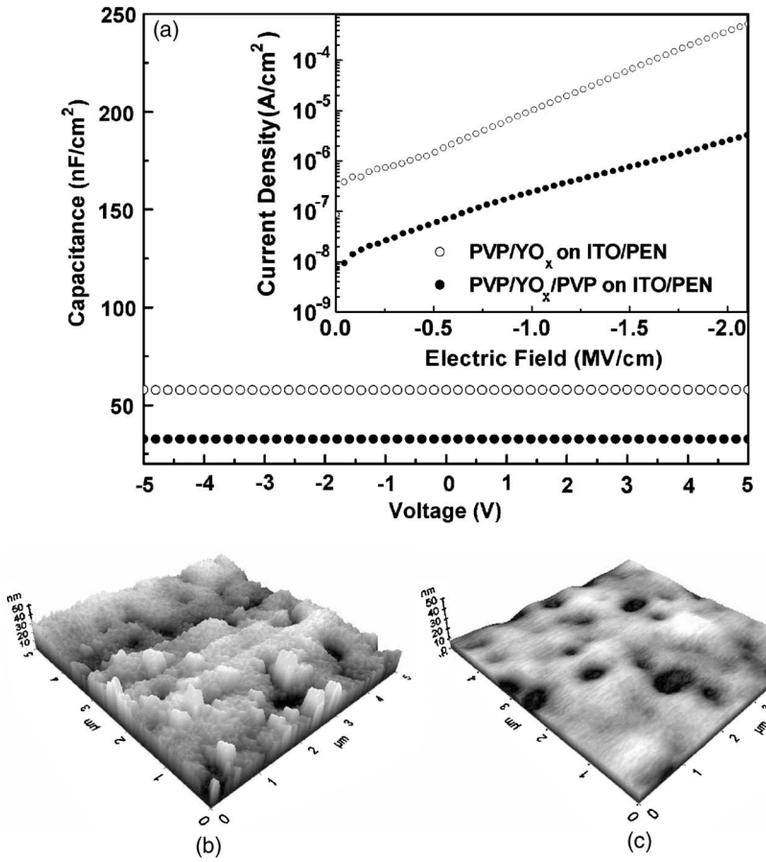

Figure 2. (a) Plots of C–V and (inset) J–E characteristics measured from Au-pad/dielectric insulator/ITO/PEN substrate structures. Chosen dielectrics were PVP (45 nm)/YO_x (50 nm) and PVP (45 nm)/YO_x (50 nm)/PVP (45 nm). (b) AFM images of ITO film coated on PEN substrate and (c) PVP (45 nm) layer spin-coated on ITO/PEN substrate.

voltage (C–V) and current density–electric field J–E tests. All current–voltage (I–V) characteristics of our TFTs, test structures, and resistance-load inverters were measured with a semiconductor parameter analyzer (HP 4155C, Agilent Technologies), and C–V measurements were made with a HP 4284 capacitance meter (1 MHz) in the dark at room temperature. The surface of each layer was characterized by atomic force microscopy (AFM) (PSIA, XE-100). The sheet resistance of NiO_x films ($\sim$100 $\Omega/\square$) was determined by van der Pauw method.

Results and Discussion

Figure 2a displays the C–V and J–E (inset) characteristics of an Au/dielectric insulator/ITO structure formed on a PEN substrate, obtained from two types of hybrid dielectric layers: double [PVP (45 nm)/YO_x (50 nm)] and triple [PVP (45 nm)/YO_x (50 nm)/PVP (45 nm)]. The capacitances of PVP/YO_x and PVP/YO_x/PVP layers were measured to be about 57.5 and 33 nF/cm^2, respectively, because the triple layer is thicker than the double. In our previous report, the dielectric constant, k, of YO_x and PVP films were estimated to be $\sim$14.6 and 3.7, respectively,[13] and the present capacitances measured from the two types of hybrid layer (double and triple) are consistent with the theoretical values (57 and 32 nF/cm^2) of serially connected capacitors.

According to the J–E curve of Fig. 2a inset, the PVP/YO_x/PVP triple layer exhibits quite a good dielectric strength of $\sim$2 MV/cm based on our minimum leakage-current standard of $\sim 10^{-6}$ A/cm^2. However, the PVP/YO_x double layer on an ITO/PEN substrate showed a much higher leakage current level by about 2 orders of magnitude than that of the triple layer and showed a very low dielectric strength of less than 0.4 MV/cm. Because the dielectric strength of the double layer was $\sim$2 MV/cm with a glass substrate,[13] we suspect the roughness of the ITO/plastic substrate is responsible for the strength reduction. As mentioned in the introduction, the surface of the usual ITO/plastic substrates is relatively rough compared to that of glass substrates. The irregular rough surface of the ITO gate may cause an easy breakdown failure or a high leakage-current level during device operation unless some buffering process is employed to somewhat nullify the initial edged surfaces because many peak regions in the rough surface act as electric-field (E-field) concentration centers.[14,15] The AFM surface images for ITO/PEN (Fig. 2b) and spin-cast 45 nm thick PVP/ITO/PEN (Fig. 2c) support the J–E results of Fig. 2a. The initial ITO on PEN substrate showed very irregular and rough surface morphology with a root-mean-square (rms) roughness of 5.74 nm, which is incomparably higher than that of ITO on glass ($\sim$1.5 nm). However, such a rough surface could be remarkably smoothened after spin-casting of a PVP layer. According to the AFM image of Fig. 2c, the rms roughness appeared to be only 1.7 nm after the 45 nm PVP coating. This is because viscose PVP solution fills up the valley regions of the ITO/plastic substrate. Because the surface of high-k YO_x would follow the previous film-surface contour during deposition, we would expect that the high-k layer on a rough ITO/PEN substrate should have a much higher surface roughness than that of the YO_x deposited on PVP/ITO/PEN. As a result, the E-field concentration effects on the current leakage certainly appear greater with the PVP/YO_x double layer than with the PVP/YO_x/PVP triple layer, the latter case exhibiting much lower gate-current leakage.

Figure 3a and b show the drain current–drain voltage (I_D–V_D) curves obtained from our pentacene TFTs with the PVP/YO_x/PVP triple-layer dielectric but with NiO_x and Au for S/D electrodes, respectively. We actually fabricated the same TFTs with the PVP/YO_x double layer, but the yield was too low ($\sim$less than 5%) to show their performance. Both types of devices with triple layers demonstrate desirable TFT characteristics at an operating voltage lower than -8 V as shown in Fig. 3. The pentacene TFT with NiO_x elec-

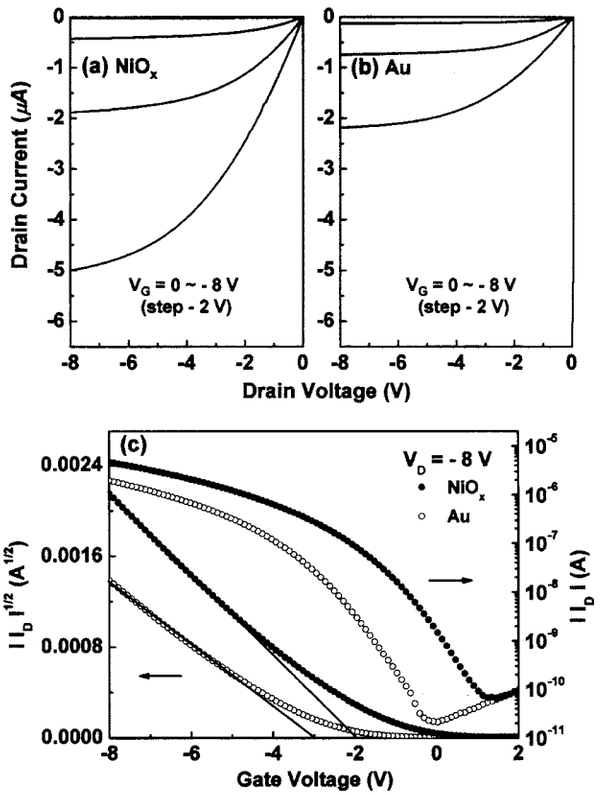

Figure 3. I_D–V_D curves obtained from our pentacene-based TFTs with (a) NiO_x and (b) Au electrodes. (c) $\sqrt{-I_D}$–V_G and $\mathrm{Log}_{10}(-I_D)$-V_G plots under a drain saturation condition ($V_D = -8$ V).

trodes apparently had a higher saturation current of −5 μA than the other TFT with Au electrodes (−2.2 μA) because the NiO_x electrode is better matched with pentacene than Au for hole injection.[16,17] The pentacene TFT with NiO_x electrode thus exhibited higher mobility of 1.37 cm^2/V s (with a lower threshold voltage of −2 V) than that of the other device with an Au electrode (0.84 cm^2/V s), and the $\sqrt{-I_D}$ vs V_G curves of Fig. 3c show the saturation mobility and the threshold voltage trends of the two devices. According to the plots of $\mathrm{log}_{10}(-I_D)$-V_G in the same figure, the on/off current ratios for the two devices were almost identical at about 5×10^4 and their subthreshold slope was again nearly identical, about 0.7 V/dec.

Anticipating low-voltage operation, we also set up two resistance-load inverters using our two pentacene TFTs (with Au and NiO_x electrodes on ITO/plastic substrates) and a load resistor (load resistance, $R_L = 22$ MΩ) (also see the inset of Fig. 4 for the inverter scheme). The inverters operated well under −8 V input (gate bias). The measured voltage gain, dV_{out}/dV_{in}, which is a parameter important to subsequent stage-switching, was ~3.7 and ~3.1 for the pentacene TFTs with NiO_x and Au electrode, respectively.

Conclusion

In summary, we have fabricated pentacene TFTs with a PVP/YO_x/PVP triple layer on ITO/plastic substrate. The PVP/YO_x/PVP layer exhibited higher dielectric strength and lower gate-current leakage than those of a PVP/YO_x double layer because the first thin PVP layer in the triple layer nullifies the irregular surface edges of ITO/plastic substrate. Our pentacene TFTs with the triple layer demonstrated excellent field-effect mobility (1.37 cm^2/V s for NiO_x electrode) and an on/off current ratio of

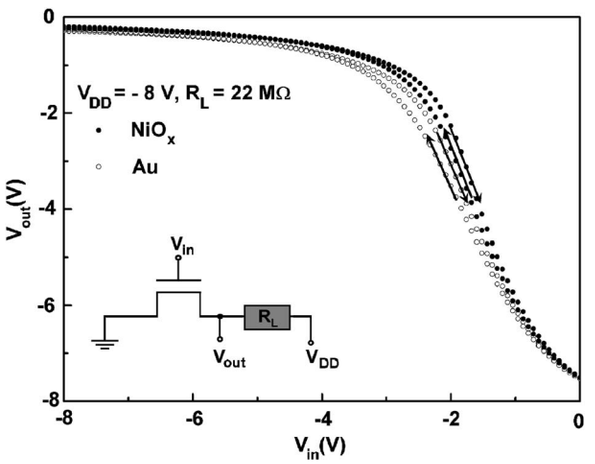

Figure 4. Circuit scheme (inset) and static behavior of our resistance-load inverters. Our two inverter sets were composed of pentacene-TFTs and a load-resistor ($R_L = 22$ MΩ).

5×10^4 at −8 V gate bias. Resistance-load inverters with our TFTs also operated well below −8 V. We thus conclude that our triple-layer approach is quite a promising and practical way to realize a flexible low-voltage high-performance OTFT and to build related circuits on ITO/plastic substrates with rough surfaces.

Acknowledgments

The authors are very appreciative of the financial support from the Korea Science and Engineering Foundation (program no. M1-0214-00-0228), LG. Philips LCD (project year 2005), and they also acknowledge support from Brain Korea 21 Project. J.H.K. acknowledges financial support from the Electron Spin Science Center at Postech, funded by KOSEF/MOST.

Yonsei University assisted in meeting the publication costs of this article.

References

1. C. D. Sheraw, L. Zhou, J. R. Huang, D. J. Gundlach, T. N. Jackson, M. G. Kane, I. G. Hill, M. S. Hammond, J. Campi, B. K. Greening, J. Francl, and J. West, *Appl. Phys. Lett.*, **80**, 1088 (2002).
2. L. Zhou, A. Wanga, S.-C. Wu, J. Sun, S. Park, and T. N. Jackson, *Appl. Phys. Lett.*, **88**, 083502 (2006).
3. S. D. Vusser, S. Steudel, K. Myny, J. Genoe, and P. Heremansa, *Appl. Phys. Lett.*, **88**, 162116 (2006).
4. R. Rotzoll, S. Mohapatra, V. Olariu, R. Wenz, M. Grigas, K. Dimmler, O. Shchekin, and A. Dodabalapur, *Appl. Phys. Lett.*, **88**, 123502 (2006).
5. C. D. Dimitrakopoulos, S. Purushothaman, J. Kymissis, A. Callegari, and J. M. Shaw, *Science*, **283**, 822 (1999).
6. Y. Liang, G. Dong, Y. Hu, L. Wang, and Y. Qiu, *Appl. Phys. Lett.*, **86**, 132101 (2005).
7. L. Majewski, R. Schroeder, and M. Grell, *Adv. Mater. (Weinheim, Ger.)*, **17**, 192 (2005).
8. M. Halik, H. Klauk, U. Zschieschang, G. Schmid, C. Dehm, M. Schütz, S. Maisch, F. Effenberger, M. Brunnbauer, and F. Stellacci, *Nature (London)*, **431**, 963 (2004).
9. Y. D. Park, D. H. Kim, Y. Jang, M. Hwang, J. A. Lim, and K. Cho, *Appl. Phys. Lett.*, **87**, 243509 (2005).
10. M. H. Yoon, H. Yan, A. Facchetti, and T. J. Marks, *J. Am. Chem. Soc.*, **127**, 10388 (2005).
11. Y. Jang, D. H. Kim, Y. D. Park, J. H. Cho, M. Hwang, and K. Cho, *Appl. Phys. Lett.*, **88**, 072101 (2006).
12. S. Y. Yang, S. H. Kim, K. Shin, H. Jeon, and C. E. Park, *Appl. Phys. Lett.*, **88**, 173507 (2006).
13. D. K. Hwang, K. Lee, J. H. Kim, S. Im, C. S. Kim, H. K. Baik, J. H. Park, and E. Kim, *Appl. Phys. Lett.*, **88**, 243513 (2006).
14. C. Wang, L. Fang, G. Zhang, D. M. Zhuang, and M. S. Wu, *Thin Solid Films*, **458**, 246 (2004).
15. K. Ueno, S. Abe, R. Onoki, and K. Saiki, *J. Appl. Phys.*, **98**, 114503 (2005).
16. J. Lee, D. K. Hwang, J.-M. Choi, K. Lee, J. H. Kim, S. Im, J. H. Park, and E. Kim, *Appl. Phys. Lett.*, **87**, 023504 (2005).
17. K. Lee, J. H. Kim, and S. Im, *Appl. Phys. Lett.*, **88**, 023504 (2006).