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Improving Resistance to Gate Bias Stress in Pentacene TFTs with Optimally Cured Polymer Dielectric Layers

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We report on the insulator charging effects of poly-4-vinylphenol (PVP) gate dielectric on the reliabilities of pentacene thin-film transistors (TFTs). Our PVP films were prepared by spin coating and subsequent curing at various temperatures (155, 175, and 200°C). Evaluated using Au/PVP/p^+-Si structures, the dielectric strength of PVP films cured at 175°C was superior to those of the other PVP films cured at different temperatures. Although the field mobility (~0.13 cm^2/V s) obtained from a TFT with PVP film cured at 200°C appeared higher than that (~0.07 cm^2/V s) from the device with 175°C-cured polymer film, the TFT prepared at 200°C revealed a low on/off current ratio of less than 10^4 due to its high off-state current and a higher sensitivity to gate bias stress. The unreliable behavior is due to the dielectric charging caused by gate electron injection. We thus conclude that there are some optimal PVP-curing conditions to improve the reliability of pentacene TFT.
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Organic thin-film transistors (OTFTs) have been extensively studied over the last few decades, and the performance of these devices has made consistent progresses. Electronic applications such as integrated circuits[1-4] and active matrix displays[5-8] have recently been demonstrated using OTFTs by several groups. The best device performance of OTFTs has been typically obtained with high-quality inorganic gate dielectrics and noble metal source-drain (S/D) contacts.[1,6,9,10] To make use of the full advantages of OTFTs, namely, large area coverage, mechanical flexibility, and low-cost processing, it is necessary to employ polymer gate dielectric materials coated using solution processes. OTFTs with polymer gate dielectrics have thus been reported, and some of them exhibited quite a good electronic performance comparable to those with inorganic gate dielectric materials.[11-14] Poly-4-vinylphenol (PVP) is one of the popular gate materials. OTFTs with PVP gate dielectric and opaque noble-metal S/D contacts displayed a good performance with a field effect mobility of ~0.1 cm^2/V s and an on/off ratio of over 10^5.[12,13] However, the charging capacitances (or dielectric capacities) of the polymer gate dielectric are still inferior to those of inorganic dielectric materials. Moreover, sensitivity to gate bias stress in OTFTs with the polymer dielectric, resulting in threshold voltage change depending on the direction of gate voltage sweeping, has been often found and reported.[12] Few studies were reported on the reasons of the threshold voltage shift or of the unreliable behavior.[15] Hence, no report has been found on optimum PVP curing conditions for cross-linking of polymer chains, which may substantially influence the electrical properties of polymer gate dielectric films and further influence the reliability of the OTFTs with polymer gates.

In the present study, we have fabricated pentacene TFTs with a PVP dielectric and NiO_x S/D electrode, systematically varying PVP curing temperatures to achieve more reliable gate behavior from the pentacene-based TFTs with polymer dielectric layers.

Experimental

Prior to spin-coating of a PVP film on indium-tin oxide (ITO) glass, the glass was cleaned with acetone, ethanol, and deionized water in that order. The thickness and sheet resistance of the ITO films were 79 nm and 30 Ω/□. PVP films were then prepared from solution of PVP and poly(melamine-*co*-formaldehyde), as a cross-linking agent, in propylene glycol monomethyl ether acetate (PGMEA), by spin-coating and subsequent cross-linking (curing) at different temperatures (155, 175, and 200°C) for 30 min in a vacuum oven. Final thickness of the PVP films was approximately 650 nm as measured by a surface profiler (Alpha-Step IQ). Pentacene channels and semitransparent S/D NiO_x films were then sequentially patterned on the PVP layer through shadow masks at a substrate temperature of 20°C [room temperature (RT)] by thermal evaporation in a vacuum chamber that had been in a base pressure of 1×10^{-6} Torr. The thermal deposition rate was fixed to 1 Å/s for the pentacene (Aldrich Chemical Co., ~99% purity) and 30 Å/s for the evaporation of NiO powder (99.97% purity). The thickness of pentacene and NiO_x films was 50 and 100 nm, respectively, as monitored by a quartz crystal oscillator and confirmed by ellipsometry. The nominal channel length and width of our TFTs were 90 and 500 μm, respectively. (For a schematic cross-sectional view of our TFT, see Fig. 3b.)

All current-voltage (*I–V*) measurements for our TFTs were performed with a semiconductor parameter analyzer (Agilent 4155C), and the electrical properties of the PVP films were also evaluated from capacitance-frequency (*C–f*) and current density-electric field (*J–E*) measurements with Au/spin-coated PVP/p^+-Si structure. The *C–f* measurements were made with an ac impedance analyzer (HP 4192A) in the dark at RT. The sheet resistance of NiO_x films was determined by Hall measurements. Our 100-nm-thick NiO_x electrode presented quite a low sheet resistance of ~100 Ω/□. It is highly probable that our semitransparent NiO_x is off-stoichiometric and is in oxygen-deficient Ni-rich state as well. More details on the thermally evaporated NiO_x electrodes have recently been reported elsewhere.[16,17]

Results and Discussion

Figure 1 exhibits *C–f* and *J–E* (inset) characteristics as measured to observe the dielectric capacitance and strength from Au/PVP/p^+-Si structures prepared at varied curing temperatures (155, 175, and 200°C). The capacitance of 650-nm-thick PVP film cured at 175°C was measured to be about 5.3 nF/cm^2 (which has not been much varied with frequency), while those of PVP films cured at 155 and 200°C were 4.7 and 5.0 nF/cm^2, respectively. According to the capacitance data, the dielectric constant, *k*, of PVP films cured at 155, 175, and 200°C were estimated to range from 3.5 to 3.9, which are similar to the values reported by Halik et al.[11-13] The 650-nm-thick PVP film cured at 175°C appeared to have the highest dielectric strength of more than ~1.5 MV/cm, while the polymer film cured at 200°C showed one order of magnitude lower strength (or higher leakage current), and the other cured at 155°C could not accomplish the role of dielectric layer due to its very high leakage current. The heat-treatment after spin-coating is generally conducted at a temperature higher than glass transition temperature (T_g) by 20–30°C for reducing the free volume formed inside the PVP layer during spin-coating. Furthermore, the treatment at the same temperature over T_g facilitates the polymer chains to move freely and to

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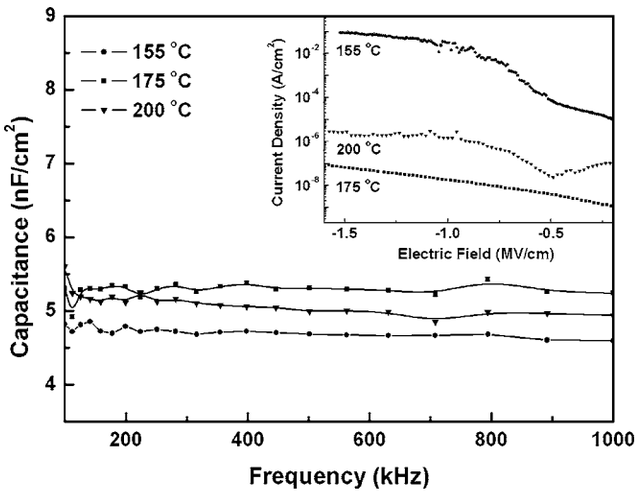

Figure 1. Plots of *C–f* and *J–E* (inset) characteristics measured from the 300-μm-diam Au/650-nm-thick PVP/heavily doped p^+-Si structures.

be effectively cross-linked. Hence, conformational transition occurs to make the PVP films more compact and less defective. Because the T_g of PVP is known to be 151°C, the observed high leakage current from the PVP films cured at 155°C is understandable. However, the leakage difference between the PVP samples cured at 175 and 200°C is not clearly understood. [Fourier transform infrared (FTIR) measurements were tried on those two PVP samples, but no signature to indicate the difference was found.] It is presumed that other factors, such as the weight ratio between cross-linking agent [poly (melamine-*co*-formaldehyde)] and PVP (1:2 in our case), and choice of solvent, may have influenced the conformation of PVP films, but it could be experimentally hard to find an optimum ratio among the chemicals. In the present work, curing at 175°C seems to be an optimum cross-linking condition for our chemically modified PVP dielectric layer.

Figure 2a and b displays the drain current–drain voltage ($I_D - V_D$) curves of our pentacene OTFTs with two PVP gate dielectric films cured at 175 and 200°C, respectively. The *I–V* curves were obtained after ten times of repeated voltage sweep, so that we might expect to observe somewhat stabilized *I–V* behavior. The $I_D - V_D$ curves of our pentacene OTFTs employing the Ni-rich NiO_x

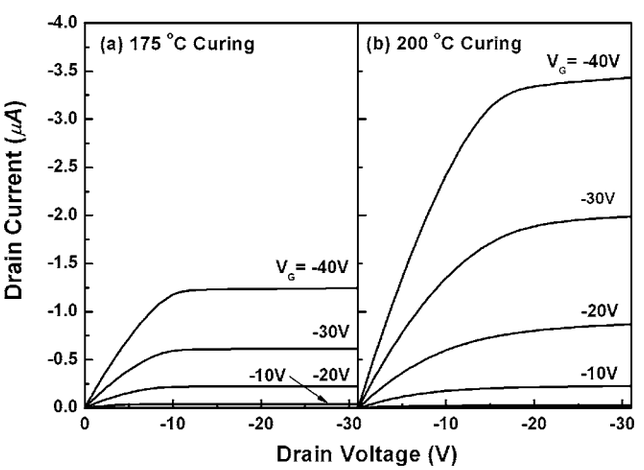

Figure 2. Drain current-voltage (I_D–V_D) curves obtained (after ten-times-repeated voltage sweep) from our OTFTs fabricated with PVP gate films cured at (a) 175 and (b) 200°C.

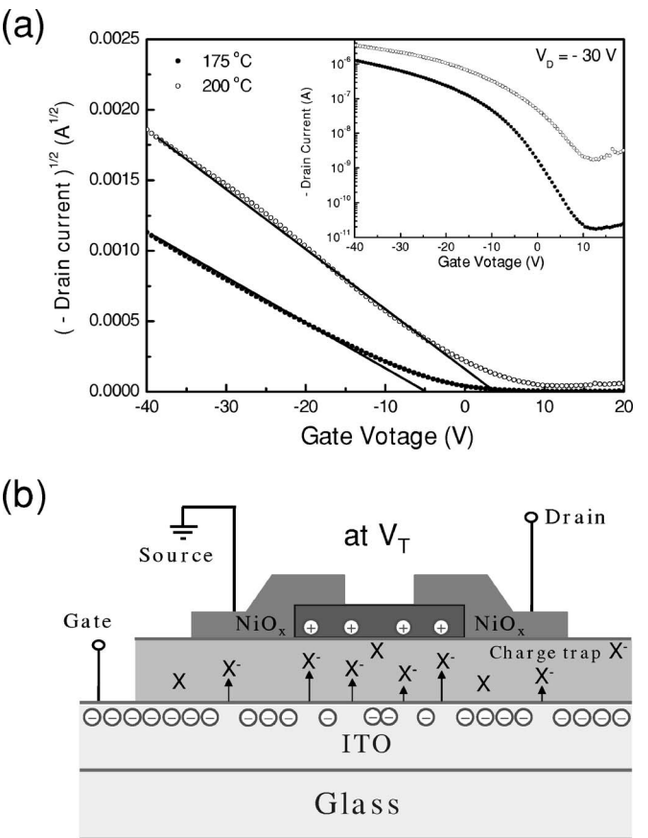

Figure 3. (a) $\sqrt{-I_D} - V_G$ and $\log_{10}(-I_D) - V_G$ (inset) plots to evaluate the field effect mobilities and the on/off behavior of the two OTFTs with PVP gate films cured at 175 and 200°C ($V_D = -30$ V). All the plots were obtained from the OTFTs that had gone through ten gate voltage sweeps. (b) A schematic cross section of our pentacene-based TFT with the PVP dielectric that has a density of defects to be negatively charged by electrons injected from an ITO gate electrode.

electrode and PVP gate dielectric show typical current saturation at high drain voltages. A maximum saturation current (I_{DSAT}) of ~1.2 μA for the OTFT prepared at 175°C was achieved under a gate bias (V_G) of −40 V, but it seems to increase with curing temperature. For the device prepared at 200°C, I_{DSAT} was measured to be about 3.4 μA under the same voltage sweep condition.

According to Fig. 3a, the field effect mobilities of two devices prepared at 175 and 200°C were estimated to 0.07 and 0.13 cm^2/Vs, respectively, based on the slope of the $\sqrt{-I_D} - V_G$ plot (under current saturation condition). These results simply reflected the I_{DSAT} data of Fig. 2a and b. However, in the aspects of on/off current ratio, the device with the higher mobility was found to be inferior to the other one prepared at 175°C [see the inset of Fig. 3, $\log_{10}(-I_D) - V_G$ plot]. The former device prepared at 200° showed much higher off-state current ($I_D \sim 2$ nA, on/off current ratio ~10^3) than the latter which exhibited only ~10 pA (on/off ratio ~10^5). It is certainly due to the higher gate leakage current from the PVP dielectric of the former device. (See the inset of Fig. 1 to check the gate leakage difference of about 2 orders of magnitude between 200 and 175°C PVP samples.) Because the pentacene channel layers for the two OTFTs were simultaneously deposited on our spin-coated PVP films cured at 175 and 200°C in the same chamber, and also because the root-mean-square surface roughness of the two PVP layers was almost the same (according to atomic force microscopy results), we suspect that only the curing temperatures have caused all the performance differences, determining the

intrinsic structures and properties of the polymer dielectrics. It is probable that 200°C-prepared PVP films contain relatively higher density charge-traps or defects which become negatively charged (by trapping electrons injected from gate electrode), as shown in the schematic TFT cross section of Fig. 3b. The I_{DSAT} value is proportional to the square of the effective gate-source voltage swing according to the following equation

$$I_{DSAT} = \frac{WC_i}{2L}\mu(V_G - V_T)^2 \quad [1]$$

where C_i is the gate dielectric capacitance per unit area (5.3 nF/cm^2), μ is the field effect hole mobility, V_T is the threshold voltage (usually negative), and W and L are the channel width and length, repectively.[18] If the threshold voltage of OTFT with p-channel appears more positive (or less negative), the I_{DSAT} increases according to Eq. 1 (an operating gate bias, V_G, for hole accumulation is always negative). Positive V_T and high off-state current are due to negatively charged traps inside the polymer gate dielectric. The presence of the high-density negative traps in the dielectric layer causes hole (positive charge) accumulation to easily occur in the channel/gate interface and hence, earlier turn-on with more positive V_T is expected. Then relatively higher saturation current can be obtained in this situation than in the case of OTFTs with less negative traps. Simultaneously, high off-state leakage current is also observed due to the traps. The $\sqrt{-I_D} - V_G$ characteristics of Fig. 3a clearly show such V_T difference in our devices with the two PVP layers prepared at 175 and 200°C. While the threshold voltage of OTFT prepared at 175°C was −5 V, that of the other device was +3.2 V. Therefore, it is understandable that OTFT prepared at 200°C shows a relatively large saturation current according to Eq. 1 and large off-state current as well.

The evidences of the presence of the negative charges trapped inside the 200°C-prepared PVP were more clearly presented at the $\sqrt{-I_D}$ vs V_G and $\log_{10}(-I_D)$–V_G plots of Fig. 4a and b, obtained by repetitively sweeping the OTFTs prepared at 175 and 200°C in our measurement gate voltage range (−40 to 20 V). In the case of OTFT using PVP gate dielectric films cured at 175°C, the on/off current ratio was not much varied and the threshold voltage moved to the positive side from −6.2 to −1.7 V until the gate voltage sweep was repeated up to 30 times. The device using PVP gate dielectric films cured at 200°C showed that the on/off current ratio considerably decreased with the repetitive gate voltage sweep while the I_D current level continually increased. The threshold voltage moved to the very much positive side (from −6.6 to 13.3 V) in this case. It is presumed that a higher density of defects are present in the polymer gate dielectric cured at 200°C than in the other cured at 175°C and continually traps the electrons injected from ITO gate electrode under the electric fields applied during the repeated voltage sweep. In fact, the PVP films cured at 200°C have appeared more vulnerable to the voltage stress from gate bias than those cured at 175°C, as shown in the results from Fig. 1, Fig. 3a, and Fig. 4b. It is thus natural to consider that the injected electrons from the ITO gate electrode may more easily be admitted to the 200°C-cured polymer, being coupled with the defects in the polymer. We thus conclude that the PVP films cured at 175° are more optimum to be dielectric layers for reliable OTFTs than those cured at 200°C.

Conclusions

We have fabricated pentacene TFTs with PVP gate dielectric layers cured at two different temperatures: 175 and 200°C. According to *C–f* and *J–E* characteristics obtained from Au/PVP/p$^+$-Si structures, optimum electrical properties were observed at the PVP film cured at 175°C, of which the dielectric constant and strength were measured to be about 3.9 and more than 1.5 MV/cm, respectively. Under repetitive V_G sweeping, not only the saturation current but also the off-state leakage current of the OTFT with PVP film cured at 200°C were found to increase, and its threshold voltage moved to more positive side while those of the other device with the PVP

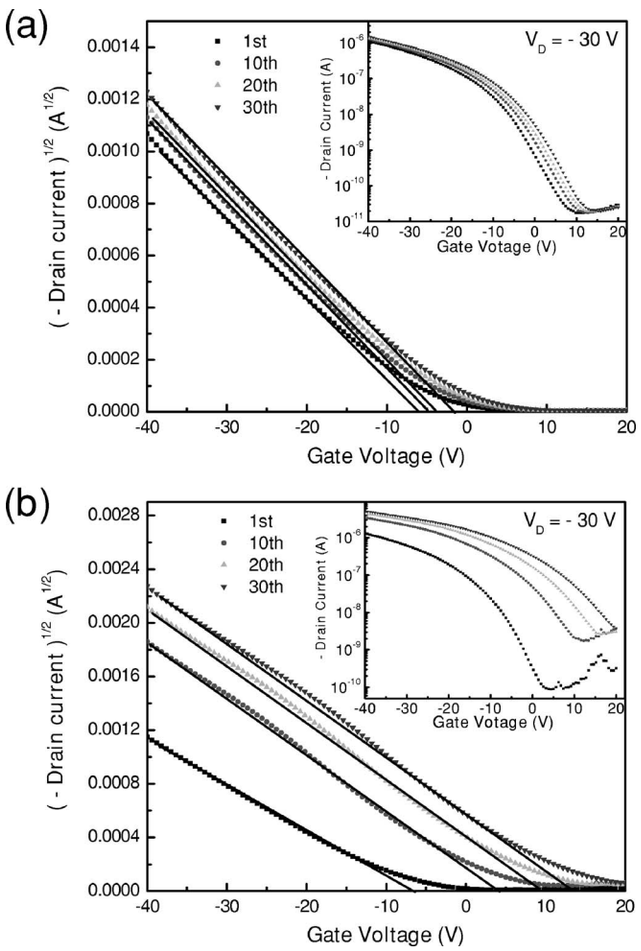

Figure 4. $\sqrt{-I_D} - V_G$ and $\log_{10}(-I_D)$–V_G (inset) plots obtained with repetitive gate voltage sweep (up to 30 times) from our OTFTs fabricated using PVP gate films cured at (a) 175 and (b) 200°C.

cured at 175°C were not much varied. This is because insulator-charging phenomena occurred due to the presence and accumulation of negative-charged defects inside our polymer gate dielectric; those defects cause both early turn-on and a low on/off current ratio in the device. It is concluded that the PVP films cured at 175°C are determined to be optimum dielectric layers for more reliable OTFTs with a field mobility of 0.07 cm^2/Vs and on/off ratio of 10^5.

Acknowledgments

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