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Polymer/YO_x Hybrid-Sandwich Gate Dielectrics for Semitransparent Pentacene Thin-Film Transistors Operating Under 5 V**

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Organic thin-film transistors (OTFTs) have been extensively studied over the last few decades and have become prominent in the future development of organic electronics, as exemplified by drivers for flat-panel displays, low-end smart cards, and electronic identification tags.[1–3] Of the many OTFTs, pentacene-based ones have attracted most attention, since pentacene-based TFTs often exhibit a reasonably high field-effect mobility of more than 1 $cm^2\,V^{-1}\,s^{-1}$, demonstrating their potential for practical applications.[4–6] However, conventional OTFTs, including pentacene-based ones, need more than 15 V for gating and charge-transport operation to achieve desirable characteristics. Very recently, low-voltage-driven OTFTs have been reported for more advanced applications, in which high-dielectric-constant (high-*k*) metal oxides (Ta_2O_3, TiO_2, etc.)[7–10] are adopted as gate insulators, or ultrathin gate dielectrics are used, such as self-assembled monolayers (SAMs)[11,12] and thin polymers.[13,14] Conventional high-*k* inorganic gate dielectric films are generally thick (typically more than ca. 100 nm) to avoid serious gate leakage current[12] and are not suitable for direct growth of an organic semiconductor channel owing to their highly hydrophilic surfaces, which are less compatible with the growth of organic crystals, probably undergoing undesirable interface interactions with organic materials. On the other hand, ultrathin organic gate dielectrics with high resultant capacitance possess good surface conditions (more hydrophobic and smoother surface) for the accommodation of an organic semiconductor channel but are still problematic due to their structural imperfections, including pinholes generated during deposition processes.[9,13,14] One way to circumvent the aforementioned drawbacks of inorganic high-*k* and ultrathin organic dielectrics is to stack an organic layer on a high-*k* inorganic film, hence selectively combining the advantages of the two gate materials.

In the present Communication, we report on the fabrication and characterization of semitransparent pentacene-based TFTs with thin poly(4-vinylphenol) (PVP)/high-*k* yttrium oxide (YO_x) sandwich gate dielectrics, and alternatively with thermally evaporated semitransparent NiO_x source/drain (S/D) electrodes. Our pentacene TFTs with PVP (45 and 70 nm)/YO_x (100 nm) layers exhibited excellent device performance under low-driving-voltage conditions (less than –5 V) with decent field-effect mobilities (maximum 0.83 $cm^2\,V^{-1}\,s^{-1}$), a low threshold voltage of –1 V, and on/off current ratios of ca. 10^4. We also demonstrate resistance-load inverters operating below –5 V with a load resistance (R_L) of 22 MΩ connected to our pentacene TFTs. These inverters exhibited a sizeable voltage gain of ca. 3.0 with hysteresis on the order of 0.5 V.

Figure 1a and b show, respectively, the schematic cross-sectional and photographic plan views of our pentacene TFTs, placed on the emblem of our institute. Although the S/D electrode regions appear darker than the pentacene channel or dielectric layer regions, we can still identify the emblem features printed on the paper. Our 100 nm thick NiO_x electrode exhibited a transmittance of 30–40 % in the visible range but quite a low sheet resistance of ca. 100 Ω/□ when it was deposited on Corning 7059 glass. It is highly probable that our semitransparent NiO_x is off-stoichiometric and is in an oxygen-deficient Ni-rich state as well. More details on the thermally evaporated NiO_x electrodes have been reported elsewhere.[15–17]

Figure 2a and b display the capacitance–voltage (*C–V*) and current-density–electric-field (*J–E*) characteristics of Au / insulator / indium tin oxide (ITO) structures with various dielectric insulators, that is, a single polymer (PVP) layer, a single YO_x layer, and two PVP/YO_x double layers. The capacitance of the 45 nm thick single PVP layer could not be measured because of its high leakage current but those of the 100 nm thick YO_x and 70 nm thick PVP layer films were measured to be about 129 and 47.3 $nF\,cm^{-2}$, respectively. According to the capacitance data, the dielectric constant, *k*, of the YO_x and

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ADVANCED MATERIALS

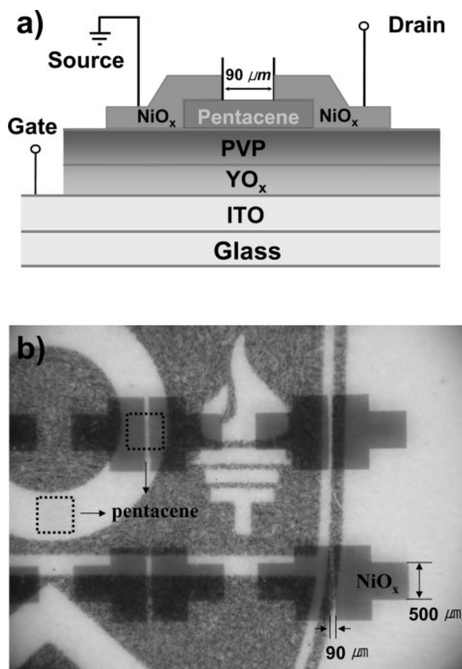

Figure 1. a) Schematic cross section of our pentacene-based TFTs (channel length, $L = 90$ μm, width, $W = 500$ μm). b) Photographic plan view of our TFT array placed on our university emblem. The dotted squares indicate the pentacene regions. ITO: indium tin oxide.

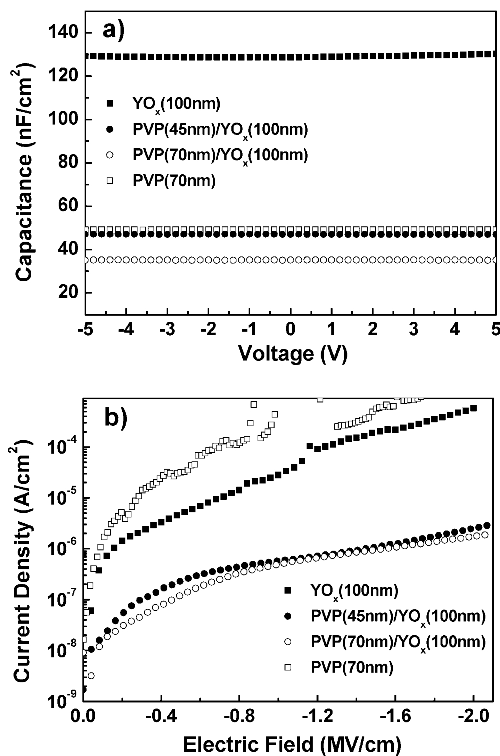

Figure 2. Plots of a) *C–V* and b) *J–E* characteristics measured for 300 μm diameter Au dot/dielectric insulator/ITO structures. Chosen dielectrics were YO_x (100 nm), PVP (70 nm), and thin and thick PVP/YO_x double-layer combinations (45 nm/100 nm and 70 nm/100 nm, respectively).

PVP films were estimated to be 14.6 and 3.7, respectively. (According to the literature, stoichiometric crystalline Y_2O_3 shows a k of 17–20 when the oxide films are annealed at a temperature higher than 450 °C[18] and k for PVP is similar to the previously reported values.[5,6]) Although the composition of our oxide films deviated somewhat from the ideal bulk stoichiometry and the oxides would be rather amorphous due to room temperature processing, our YO_x films must possess quite a high dielectric constant. When we measured the stoichiometry of our oxide by Rutherford backscattering spectrometry (RBS), it was identified as YO_3. The thin double layers of PVP (45 nm)/YO_x (100 nm) and PVP (70 nm)/YO_x (100 nm) exhibited quite high capacitance values (47.1 and 35.2 nF cm^{-2}, respectively), which are close to the theoretical values for serially connected capacitor layers.

According to the *J–E* curve in Figure 2b, the individual YO_x (100 nm) and PVP (70 nm) single layer films turned out to be inadequate as dielectric layers, exhibiting very high leakage current. Of course, the 45 nm thick PVP single layer showed much higher leakage current (not shown here). However, our double layers exhibited quite a good dielectric strength of ca. 2 MV cm^{-1}, based on our minimum leakage current standard of ca. 10^{-6} A cm^{-2}. Since the leakage current paths of YO_x and PVP films differ, it is likely that our organic/inorganic double-layer films should have a much improved dielectric strength while the single-layer films appeared rather vulnerable, failing easily under the same applied electric field.

The X-ray diffraction (XRD) spectra of Figure 3a and b show that the crystallinity of the active pentacene channel is influenced by the surface conditions of the substrate materials. While the pentacene film deposited on the YO_x layer exhibited no reflection peaks (which indicates that its phase is almost amorphous), the film grown on the PVP layer showed a good crystalline quality, as judged by the number and intensity of resolvable diffraction peaks. As mentioned at the beginning, the dielectric surface conditions such as roughness and chemical state influence the growth of the pentacene channel layer.[19–22] According to Figure 4a and b, the root-mean-square (rms) surface roughness of 100 nm thick YO_x film on ITO glass was about 1.83 nm but improved to 0.7 nm when the 45 nm thin PVP dielectric film was deposited by spin-coating. (This roughness improvement obtained for both 45 nm and 70 nm thin PVP films was found to differ slightly in rms value because the rms value for 70 nm PVP coating was 0.62 nm (not shown here).) Viscous PVP solutions must have filled up the valley regions on the YO_x surface during the spin-coating. Besides improving the dielectric surface profile, our cross-linked PVP layer also changed the chemical state (surface energy) of the dielectric surface from hydrophilic to more hydrophobic, as experimentally proven in the contact angle measurements (see Figs. 4c,d). The contact angle measured on the 100 nm thin bare YO_x film was about 24° while it changed to about 68° on PVP film (regardless of the PVP thickness). As a result, the pentacene grown on the PVP-coated, smooth YO_x layer exhibited a good crystalline phase while the other one grown on the hydrophilic, rough

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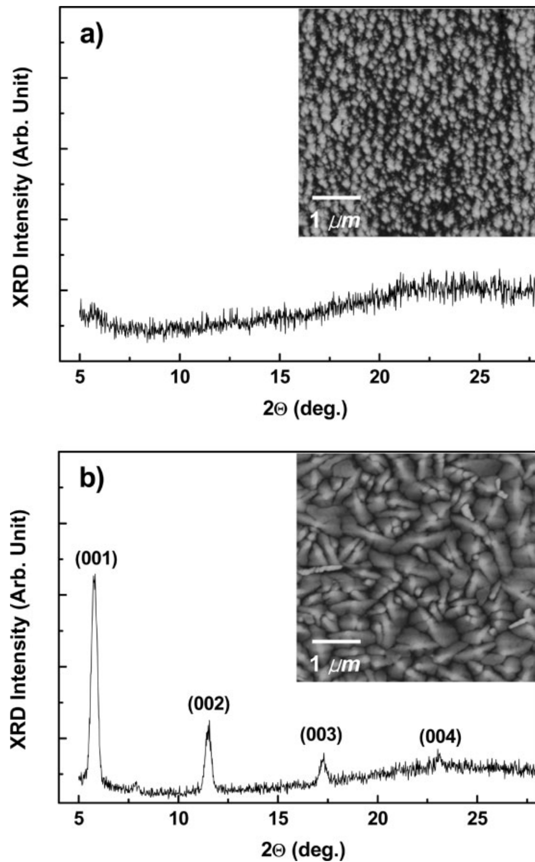

Figure 3. XRD spectra and atomic force microscopy (AFM) images obtained from pentacene films deposited on a) a 100 nm thick YO_x single layer and b) a PVP (45 nm) / YO_x (100 nm) double layer.

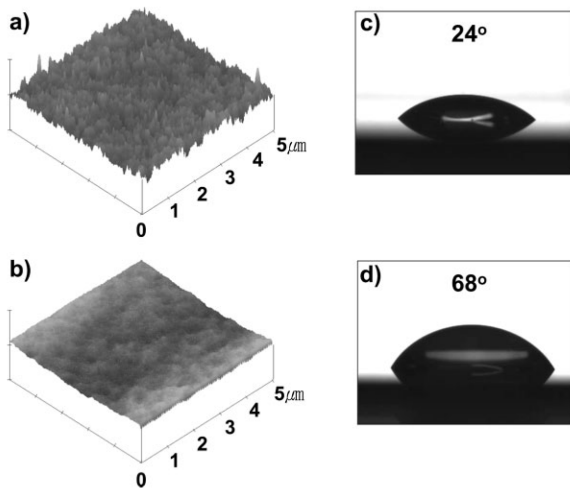

Figure 4. a,b) AFM images obtained from a 100 nm thick YO_x single layer (a) and a PVP (45 nm)/YO_x (100 nm) double layer (b). c,d) Contact angle data measured on the surfaces of bare YO_x (c) and a PVP/YO_x double layer (d). We used deionized water for the measurements.

YO_x layer appeared amorphous. Atomic force microscopy (AFM) images shown in Figure 3a and b supported the XRD results. As expected, the pentacene film on the bare YO_x layer shows very poor surface morphology, but well-formed dendritic grains are observed for the film deposited on the PVP-coated YO_x layer. Consequently, our scheme of fabricating a pentacene TFT with a double dielectric layer with the PVP on top of the YO_x could be an effective means of achieving a high-quality pentacene channel.

Figure 5a and b show the drain-current–drain-voltage curves (I_D–V_D) obtained from our pentacene-based TFTs with the PVP/YO_x double-layer gate dielectric of two different thickness combinations: thin (PVP/YO_x = 45 nm/100 nm)

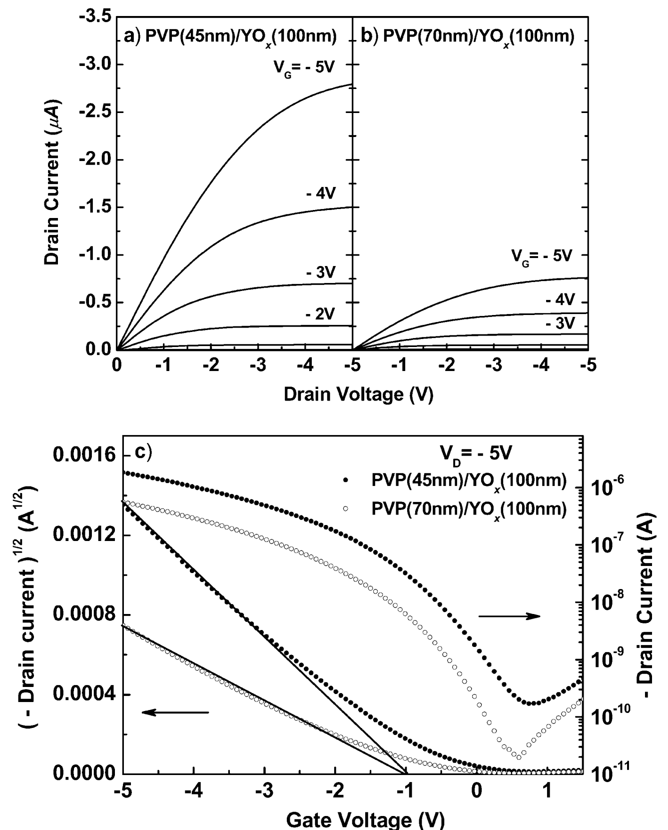

Figure 5. a,b) Drain current versus drain voltage (I_D–V_D) curves obtained from our pentacene-based TFTs with PVP (45 nm)/YO_x (100 nm) (a) and PVP (70 nm)/YO_x (100 nm) (b) dielectric combinations. c) $\sqrt{-I_D}$ versus gate voltage, V_G, and $\text{Log}_{10}(-I_D)$ versus V_G plots under drain saturation conditions (V_D = –5 V).

and thick (PVP/YO_x = 70 nm/100 nm). Both types of devices successfully demonstrated desirable TFT characteristics at an operating voltage lower than –5 V. Maximum saturation current of ca. 2.8 μA was achieved under a gate bias (V_G) of –5 V from the OTFT with the thin double-layer dielectric, while about 0.76 μA was achieved from the other OTFT with the thick double-layer dielectric, which must have a lower capacitance than that of the thin double-layer dielectric.

Field-effect mobilities were determined from $\sqrt{-I_D}$ versus V_G curves, as shown in Figure 5c. According to the saturation-mobility estimate based on the slope of the curves, the pentacene TFT fabricated with the thin double-layer dielectric has

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a higher mobility (0.83 $cm^2 V^{-1} s^{-1}$) than the device with the thick double-layer dielectric, which still has a decent mobility of 0.4 $cm^2 V^{-1} s^{-1}$. The threshold voltages for the two pentacene TFTs were similar, about –1 V, suggesting that the pentacene-channel/PVP interface states for both TFTs are not much different from each other.[23,24] According to the plots of $\log_{10}(-I_D)$ versus V_G of Figure 5c, the on/off current ratios for the two devices with thin and thick double-layer dielectrics were almost identical, about 10^4, and their subthreshold slopes were also identically close to 0.5 volts per decade. The device performance of our low-voltage-driven pentacene TFTs is comparable to or even better than previously reported cases.[7–10,14] In addition, the semitransparent NiO_x electrode employed for our TFTs can certainly lead to many notable applications in transparent electronics, which were so far out of the question in previous low-voltage-driven TFTs with opaque noble metals for S/D electrodes.

Figure 6a and b exhibit the static behavior of resistance-load inverters along with a scheme of the device (inset), which is composed of our pentacene TFT and a load resistor (load resistance $R_L = 22$ MΩ for the thin-double-layer device and 100 MΩ for the thick-double-layer device). Our inverters, as tested with the two pentacene TFTs of thin- and thick-double-layer dielectrics, operate below 5 V and the inverter response to output voltage switching is very clear between –5 V ("high") and 0 V ("low") for both cases. Some hysteresis, which has a maximum ΔV of less than 0.5 V, was observed for both devices during the inverter action, reflecting a degree of threshold voltage stability in our TFTs. The hysteresis is possibly due to mobile charges in the polymer dielectrics.[6] The measured voltage gain, dV_{out}/dV_{in}, which is a parameter important for subsequent stage switching, was ca. 3.0 and ca. 3.3 for the pentacene TFTs with thin- and thick-double-layer dielectrics, respectively. These parameters exhibit real potential of our TFTs for logic circuits operating at low voltage. Based on device and inverter performance presented above, our pentacene TFT with an organic–inorganic double-layer (sandwich) dielectric is certainly a realistic, readily usable component for low-voltage devices.

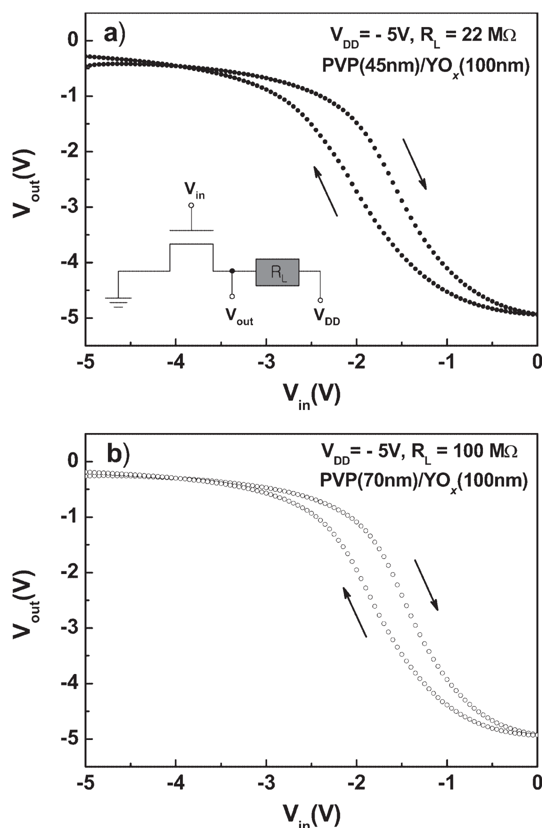

Figure 6. Static behavior of our resistance-load inverters. Our two inverter sets were composed of a pentacene TFT (with a PVP/YO_x double-layer dielectric) and a load resistor. a) TFT with PVP (45 nm)/YO_x (100 nm) dielectric and a load resistance of 22 MΩ; b) TFT with PVP (70 nm)/YO_x (100 nm) dielectric and $R_L = 100$ MΩ.

In conclusion, we have fabricated semitransparent pentacene-based TFTs and resistance-load inverters operating at a low voltage of –5 V, using thin PVP/YO_x double-layer (sandwich) dielectric films and semitransparent NiO_x S/D electrodes. The thin PVP/YO_x double layer showed quite a good dielectric strength (ca. 2 $MV cm^{-1}$) and a high capacitance (our maximum is ca. 47.1 $nF cm^{-2}$). Displaying good pentacene crystal growth or channel formation on the double-layer gate dielectrics with PVP on top, our pentacene TFTs demonstrated desirable characteristics of decent field-effect mobility (maximum 0.83 $cm^2 V^{-1} s^{-1}$) and on/off current ratio of 10^4 at –5 V gate bias. Resistance-load inverters, as tested with our TFTs, also operated below –5 V, showing a maximum voltage gain of 3.3 with some hysteresis. We thus conclude that our PVP/YO_x double layer is a promising new gate dielectric for realizing a low-operating-voltage pentacene TFT.

Experimental

Prior to the deposition of dielectric films on ITO glass, the glass was cleaned with acetone, ethanol, and deionized water, in that order. The thickness and sheet resistance of the ITO films were, respectively, 79 nm and 30 Ω/□. Subsequently, yttrium oxide (YO_x) films were deposited by electron beam evaporation using 99.999 % Y_2O_3 pellets in a vacuum chamber at room temperature (RT) (the initial base pressure was about 5×10^{-7} Torr (1 Torr $\approx 1.33 \times 10^2$ Pa) and the working pressure of O_2 gas was fixed at 1×10^{-4} Torr). The thickness of the YO_x film was set to 100 nm as monitored by a quartz crystal oscillator and the value was confirmed by a surface profiler (Alpha-Step IQ). (Our oxides were identified to be amorphous and off-stoichiometric (YO_3), characterized by XRD and 2 MeV He^{2+} RBS, respectively. The O_2 working pressure was an experimental value determined to avoid easy oxide breakdown.) PVP films were then prepared from solutions of PVP and poly(melamine-*co*-formaldehyde), as a cross-linking agent, in propylene glycol monomethyl ether acetate (PGMEA), by spin-coating and subsequent cross-linking (curing) at 175 °C for 1 h in a vacuum oven. The final thicknesses of the PVP films were approximately 45 and 70 nm as measured by the surface profiler. Pentacene (Aldrich Chem. Co., ca. 99 % purity) channels and semitransparent S/D NiO_x films were then sequentially patterned on the PVP/YO_x layers through a shadow mask on substrates at RT by thermal evaporation. The thermal deposition rate was set at 1 Å s^{-1} for the pentacene using an effusion cell (Alphaplus Co., LTE-500S) in a vacuum chamber (base pressure ca. 1×10^{-7} Torr) and 30 Å s^{-1} for the evapora-

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tion of NiO powder (99.97 % purity). The thicknesses of pentacene and NiO_x films were 50 and 100 nm, respectively, as monitored by a quartz crystal oscillator and as confirmed by ellipsometry. The nominal channel length and width were 90 µm and 500 µm, respectively.

The electrical properties of the PVP/YO_x double-layer gate dielectric films were measured on a Au/PVP/YO_x/ITO glass structure by capacitance–voltage (*C–V*) and current-density–electric-field (*J–E*) tests. All current–voltage (*I–V*) characteristics of our TFTs, test structures, and resistance-load inverters were measured with a semiconductor parameter analyzer (HP 4155C, Agilent Technologies). *C–V* measurements were made with a HP 4284 capacitance meter (1 MHz) in the dark at RT. XRD measurements were performed with monochromatic Cu Kα ($\lambda = 1.54$ Å) radiation to investigate the crystallinity of the pentacene films deposited on YO_x and PVP layers. The surface of each layer was characterized by AFM (Nanoscope IV, Digital Instruments). The sheet resistance of NiO_x films was determined to be ca. 100 Ω/□ by Hall measurements.

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