Comparative studies on the stability of polymer versus SiO_2 gate dielectrics for pentacene thin-film transistors

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(Received 30 March 2006; accepted 24 July 2006; published online 1 September 2006)

The authors report on the electrical reliabilities of poly-4-vinyl phenol (PVP) and SiO_2 gate dielectrics for pentacene thin-film transistors (TFTs). SiO_2 films were grown by dry oxidation and PVP films were prepared by spin coating and subsequent cross-linking at 175 °C for 15 min. The pentacene TFTs with the PVP cured for 15 min exhibited a large hysteresis and an abnormal drain-current increase under a gate bias stress over time, while the other TFT with SiO_2 displayed a small hysteresis but its drain current decreases with time. The hysteresis behaviors induced by PVP and SiO_2 were opposite to each other in the gate bias swing direction, due to the difference in hysteresis mechanism between the two types of TFTs. Comparing their hysteresis behavior, the authors fabricated a far more reliable pentacene TFT with PVP by extending the PVP curing time to 1 h. Our improved device with PVP exhibited no hysteresis and persistent toughness to the gate bias stress. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2345243]

Organic thin-film transistors (OTFTs) have been extensively investigated due to their potential for future organic electronic applications such as drivers for flat-panel displays, low-end smart cards, and electronic identification tags.[1–3] In particular, the pentacene-based TFTs have attracted dominant attention, since they often exhibit a considerably high hole mobility comparable to or better than the electron mobility of amorphous silicon TFTs, and already demonstrated their potentials toward organic electronic applications.[4–6] Now it is about time to solve further practical problems such as electrical reliabilities of OTFTs with pentacene active layer. The issue of electrical reliabilities is very important to any applications and it is mainly about the behavior of gate-bias-induced hysteresis and time-dependent drain-current changes under a constant gate bias or bias stress. Recently, several research groups investigated the hysteresis or bias-stress-induced instability of pentacene TFTs with SiO_2 and polymer gate dielectric films.[7–12] However, the origins of the unreliable behavior found in the two types of TFTs are still not clear at all, although the hysteresis observed from the TFT with SiO_2 is probably associated with trapped electrons at the pentacene/dielectric interface.[10] In our previous study, we reported an optimum cross-linking (curing) temperature of poly-4-vinyl phenol (PVP), leading to a more reliable gate-bias-stress-resistant PVP dielectric.[13]

In the present work, we fabricated pentacene TFTs with PVP and SiO_2 dielectrics to compare their own electric instabilities, to further examine their hysteresis mechanisms, and finally, to achieve the most reliable (i.e., hysteresis-free and stress resistant) PVP dielectrics for a pentacene-TFT.

Our SiO_2 and PVP gate dielectric films (measured capacitances: PVP=7.3 nF/cm^2 and SiO_2=17.26 nF/cm^2) were deposited on a heavily doped p-type (p^+) Si substrate. SiO_2 films (as a reference gate dielectric) were grown by dry oxidation and the final thickness of SiO_2 films was 200 nm as measured by ellipsometry. PVP films were prepared from solutions of PVP and polymelamine-co-formaldehyde, as a cross-linking agent, in propylene glycol monomethyl ether acetate, by spin coating in air ambient with a relative humidity of ~15% and subsequent cross-linking (curing) at 175 °C (Ref. 13) for 15 min and 1 h in a vacuum oven. Figure 1(a) exhibits the chemical structures of PVP and polymelamine-co-formaldehyde (cross-linking agent). Hy-

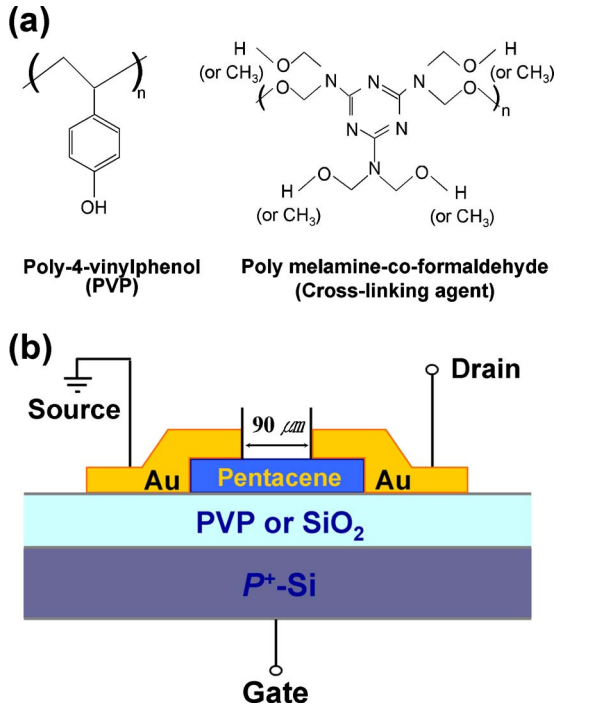

FIG. 1. (Color online) (a) Chemical structures of PVP and polymelamine-co-formaldehyde (cross-linking agent). (b) A schematic cross-sectional view of our pentacene-based TFTs (channel length L=90 μm and width W=500 μm).

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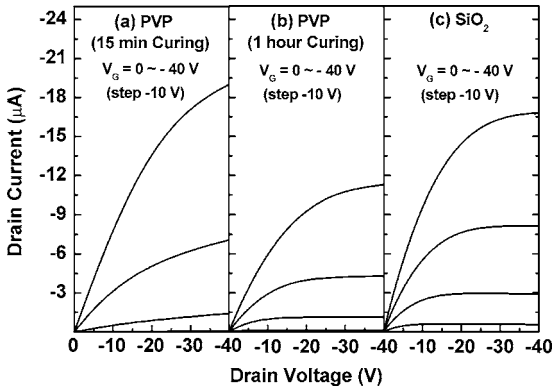

FIG. 2. Drain current-drain voltage (I_D-V_D) curves obtained from our pentacene-based TFTs with the PVP cured for (a) 15 min and (b) 1 h, and (c) from the SiO_2 dielectric layers.

droxyl groups of PVP are coupled with hydrogen or methyl groups of polymelamine-co-formaldehyde during curing processes. Through this condensation reaction, hydroxyl groups in PVP were removed and PVP films were cross-linked. The final thickness of the PVP films was approximately 470 nm as measured by the surface profiler (Alpha-Step IQ). Pentacene (Aldrich Chem. Co., ~99% purity) channels were patterned on the dielectric layers through a shadow mask by thermal evaporation at a substrate temperature of room temperature. We fixed the deposition rate to 1 Å/s for the thermal evaporation using an effusion cell (AlphaPlus Co., LTE-500S) in a vacuum chamber (base pressure $\sim 1\times 10^{-7}$ Torr). The thickness of the pentacene film was 50 nm as monitored by a quartz crystal oscillator and later confirmed by ellipsometry. The source/drain Au electrodes were finally deposited by thermal evaporation. As shown in the schematic cross-sectional view of Fig. 1(b), the nominal channel length (L) and width (W) of our pentacene TFTs were 90 and 500 μm, respectively. All current-voltage ($I-V$) characteristics of our pentacene TFTs, including the gate-bias-stress endurance, were measured in the dark and air ambient with a relative humidity of ~15% at room temperature (25 °C) with a semiconductor parameter analyzer (HP 4155C, Agilent Technologies).

Figures 2(a)–2(c) show the drain current–drain voltage curves (I_D-V_D) obtained from pentacene TFTs with PVP films cured for 15 min and 1 h, and from another pentacene TFT with the reference SiO_2 dielectric, respectively. In Fig. 2(a), the TFT with a PVP film displayed a maximum drain current of ~19 μA under a gate bias (V_G) of −40 V when cured for only 15 min, but the current probably did not saturate. When the curing continued for 1 h, the TFT exhibited good saturation behavior although the amount of drain current slightly decreased to ~12 μA. On the other hand, our reference TFT with SiO_2 dielectric exhibited good saturation as well as quite a high current of ~17 μA.

According to the $\sqrt{-I_D}-V_G$ and $\log_{10}(-I_D)-V_G$ relationships of Figs. 3(a) and 3(b), the TFT with 15 min cured PVP has a large hysteresis (threshold voltage change, $\Delta V_T = \sim 9$ V) with respect to the gate bias swing and a high off current of a few nanoamperes. The gate-swing hysteresis was observed even in the reference TFT with thermal SiO_2 although its amount was as small as ~3 V in Fig. 3(b). On the other hand, our pentacene TFT with an optimal PVP film cured for 1 h maintained its threshold voltage (V_T) at −10 V

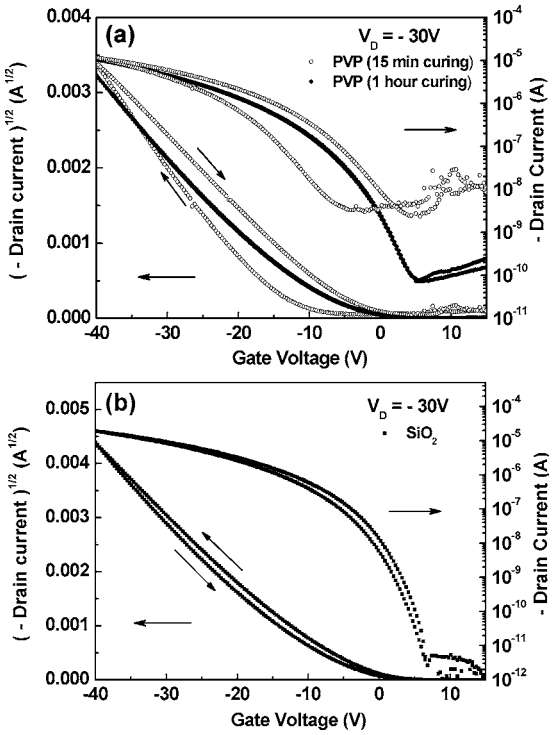

FIG. 3. $\sqrt{-I_D}-V_G$ and $\log_{10}(-I_D)-V_G$ plots obtained from our pentacene TFTs with (a) PVPs and (b) reference SiO_2 under $V_D=-30$ V.

under the same gate bias swing and showed a decent field effect mobility of 0.58 $cm^2/V\,s$, an on/off current ratio of 10^5, and a subthreshold slope (SS) of 2.5 V/decade in Fig. 3(a). The mobility and on/off ratio of our reference TFT with SiO_2 were about 0.4 $cm^2/V\,s$ and $\sim 10^6$, respectively [Fig. 3(b)]. The SS value (~1 V/decade) of the reference TFT appeared much superior to those of the TFTs with PVP. One reason for the inferior SS values (2.5~4.5 V/decade) from the OTFTs with PVP dielectrics could be because polymer dielectrics generally have "slow polarization" characteristics.[14,15]

It is interesting to note that the hysteresis directions observed from the two TFTs with immature PVP and SiO_2 are opposite to each other [see the direction arrows in Figs. 3(a) and 3(b)]. For SiO_2 dielectric films, our hysteresis results agree with a recent report by another research group. Gu *et al.* suggested that the gate-swing hysteresis was caused by electron traps (electrochemical traps such as surface hydroxyl groups[16]) at the organic-channel/inorganic-dielectric interface, where the trapping and detrapping of electrons take place during the bias swing.[10] However, in the case of the TFT with a less-cured PVP film, it is likely that the opposite-direction hysteresis is related to the slow polarization dominantly due to OH groups inside the immaturely cured PVP, where the OH groups might cause remnant dipoles during the off-to-on gate swing although it is also suggested that some mobile negative ions from internal impurities in the polymer could drift.[11] During the on-to-off swing, the I_D level thus increases and threshold voltage shifts to a smaller gate bias. The curing time of 15 min was not sufficient to cross-link PVP films, so that the polymer film might be porous and still possess some residual OH groups inside the less-cured PVP. In contrast, our long-term-cured PVP might possess only a minimal density of OH groups and internal impurities. In this case, the remnant dipole effects become

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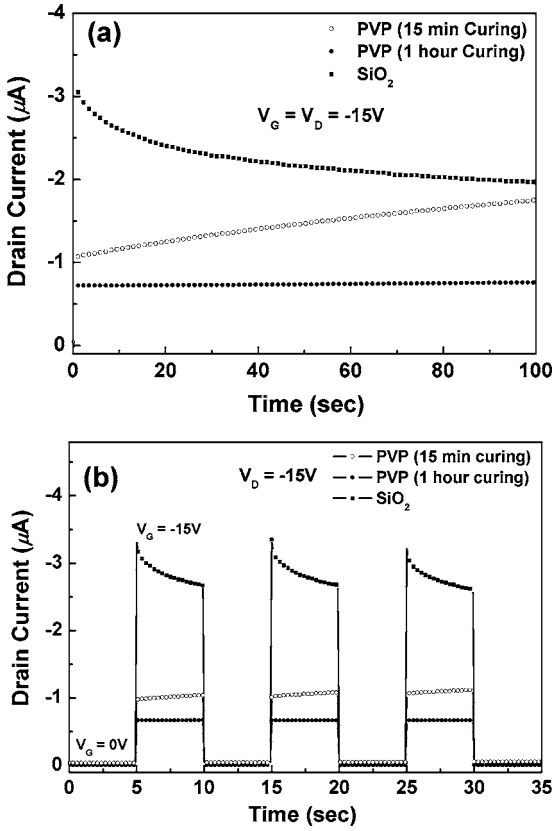

FIG. 4. Time-dependent I_D characteristics (a) under a gate bias stress of $V_G=V_D=-15$ V and (b) under $V_D=-15$ V with on-and-off gate dynamics (10 s period).

minimized. Besides, the minimal remnant dipole effects could be effectively cancelled by the aforementioned interfacial trap effects although the electron trap density could be much smaller on our less-polar PVP surface than on the polar SiO_2 surface. As a result, our TFT with fully cured PVP demonstrates the most stable, hysteresis-free I_D-V_G characteristics in Fig. 3(a).

Different hysteresis behaviors observed in our PVP- and SiO_2-type TFTs were again supported by gate bias stress experiments in Fig. 4(a). In the case of the TFT with SiO_2, I_D decreases with time, probably because the accumulated hole density gradually decreases with detrapping of electrons under a constant turn-on bias (−15 V).[10] The I_D of the TFT with the unstable PVP rather increased with time either because of the slow polarization or partly because of negative mobile ion drift toward the interface, so that more holes in pentacene might be attracted to the channel/PVP interface, making the channel more conductive. Similar results were reported by others although they thought that the above effect was only related to the dielectric surface.[12]

In Fig. 4(b), above-mentioned instabilities are somewhat dynamically expressed with the on-and-off period of 10 s and we could note few more findings from this experiment. The electron trapping and detrapping behaviors in the pentacene/SiO_2 interface appear quite reproducible during the continuous on-and-off actions, while the I_D of the TFT with the immature PVP continually and irreversibly increases. Since the speed of dipole orientation in PVP might be slow enough to result in remnant dipoles while the detrapping of the interface-trapped electrons on SiO_2 is quite fast these dynamic results are fairly understandable. Our TFT with an optimum stable PVP film does show very little change in I_D [see Figs. 4(a) and 4(b)] and we thus conclude that a sufficient curing time for PVP cross-linking is highly necessary to realize an electrically reliable pentacene TFT with a PVP dielectric.

In summary, we have fabricated pentacene TFTs with PVP and SiO_2 dielectrics to study their electrical reliabilities. The pentacene TFTs with the PVP cured for 15 min showed a large hysteresis and an abnormal drain-current increase under a gate bias stress as time elapses, while the other TFT with SiO_2 insulator displayed a small hysteresis but its drain current decreases with time. The hysteresis behaviors of the two pentacene TFTs with PVP and SiO_2 were opposite to each other with respect to the gate bias swing direction. The origins of hysteresis and stress-induced I_D changes are attributed to the remnant dipoles due to slow polarization for PVP-type pentacene TFTs and the trapping/detrapping of electrons at the channel/dielectric interface for the SiO_2 type. Based on our understanding of the origins of these instabilities, we fabricated a reliable, hysteresis-free pentacene TFT with PVP by extending PVP curing time to 1 h.

The authors are very appreciative of the financial support from KOSEF (Program No. M1-0214-00-0228) and LG Philips LCD Co. (project year 2005). They also acknowledge the support from Brain Korea 21 Project. One of the authors (J.H.K.) acknowledges financial support from the *Electron Spin Science Center* at Postech, funded by KOSEF/MOST.

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