Low-voltage high-mobility pentacene thin-film transistors with polymer/high-*k* oxide double gate dielectrics

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We report on the fabrication of pentacene-based thin-film transistors (TFTs) with poly-4-vinylphenol (PVP)/yttrium oxide (YO_x) double gate insulator films. The minimum PVP and YO_x layer thicknesses were chosen to be 45 and 50 nm, respectively. The PVP and YO_x double dielectric layers with the minimum thicknesses exhibited a high dielectric capacitance of 70.8 nF/cm^2 and quite a good dielectric strength of ~2 MV/cm at a leakage current level of $\sim 10^{-6}$ A/cm^2 while the leakage current from either PVP or YO_x alone was too high. Our pentacene TFTs with the 45 nm thin PVP/50 nm thin YO_x films operated at −5 V showing a high field effect mobility of 1.74 $cm^2/V\,s$ and a decent on/off current ratio of 10^4. Our work demonstrates that the PVP/YO_x double layer is a promising gate dielectric to realize low-voltage high-mobility organic TFTs. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2206555]

Organic thin-film transistors (OTFTs) have been extensively studied over the last few decades and developed to lead the future of organic electronics. In particular, the pentacene-based OTFTs have attracted much attention and have already demonstrated their potentials toward organic electronic applications.[1–3] However, in general, conventional OTFTs need more than 15 V for gating and charge-transport operation. Very recently, low-voltage driven OTFTs have been reported for use in more advanced applications, adopting high-*k* metal oxides (Ta_2O_3, etc.) (Refs. 4–7) as gate insulators, ultrathin gate dielectrics such as self-assembled monolayers[8,9] (SAMs) and thin polymers,[10,11] or adopting polymer electrolyte dielectrics.[12,13] Conventional high-*k* gate dielectric films are generally thick (typically, more than ~100 nm) to avoid serious gate leakage current[9] and are not quite suitable for direct growth of an organic semiconductor channel due to their highly hydrophilic surfaces that are less compatible with growth of organic pentacene, probably making some undesirable interface interaction with pentacene. On the other hand, ultrathin organic gate dielectrics with high resultant capacitance possess good surface conditions (more hydrophobic and smoother surface) to well accommodate an organic semiconductor channel but are still problematic due to their structural imperfections including pinholes generated during deposition processes.[6,10,11] One way to circumvent the aforementioned drawbacks from the inorganic high-*k* and ultrathin organic dielectrics is to stack the organic layer on the high-*k* inorganic film, hence combining the advantages from both gate materials. In the present study, we report on the fabrication and performance of pentacene-based TFTs with thin poly-4-vinylphenol (PVP)/high-*k* yttrium oxide (YO_x) double gate dielectric layers.

The sheet resistance of our cleaned indium-tin-oxide (ITO) films was 30 Ω/□. YO_x films were deposited on the ITO by electron-beam evaporation using 99.999% Y_2O_3 pellets in a vacuum chamber at room temperature (RT). The thicknesses of YO_x films were set to 50 and 100 nm as confirmed by ellipsometry. PVP films were then prepared from solutions of PVP and poly (melamine-co-formaldehyde), as a cross-linking agent, in propylene glycol monomethyl ether acetate (PGMEA), by spin coating and subsequent cross-linking (curing) at 175 °C for 1 h in a vacuum oven. The final thicknesses of the PVP films were approximately 45 and 70 nm as measured by a surface profiler. Pentacene (Aldrich Chem. Co., ~99% purity) channels were patterned on the PVP/YO_x layers through a shadow mask at a substrate temperature of RT by thermal evaporation. We fixed the deposition rate to 1 Å/s using an effusion cell (ALPHAPLUS Co., LTE-500S) in a vacuum chamber (base pressure $\sim 1 \times 10^{-7}$ Torr). The thickness of the pentacene film was 50 nm as monitored by a quartz crystal oscillator and confirmed by ellipsometry. The source/drain Au electrodes were finally deposited by thermal evaporation. As shown in the schematic cross-sectional view of Fig. 1(a), the nominal channel length (*L*) and width (*W*) of our pentacene TFTs were 90 and 500 μm, respectively.

The electrical properties of the PVP/YO_x double gate dielectric films were measured on Au/dielectric/ITO glass structures through capacitance-voltage (*C-V*) and current density-electric field (*J-E*) tests. All current-voltage (*I-V*) characteristics of our TFTs and test structures were measured with a semiconductor parameter analyzer (HP 4155C, Agilent Technologies), and *C-V* measurements were made with an HP 4284 capacitance meter (1 MHz) in the dark at RT. The surface of each layer was characterized by atomic force microscopy (AFM) (Nanoscope IV, Digital Instruments).

Figure 1(b) exhibits *C-V* and *J-E* (inset) characteristics of Au/dielectric/ITO structures, from which the dielectric ca-

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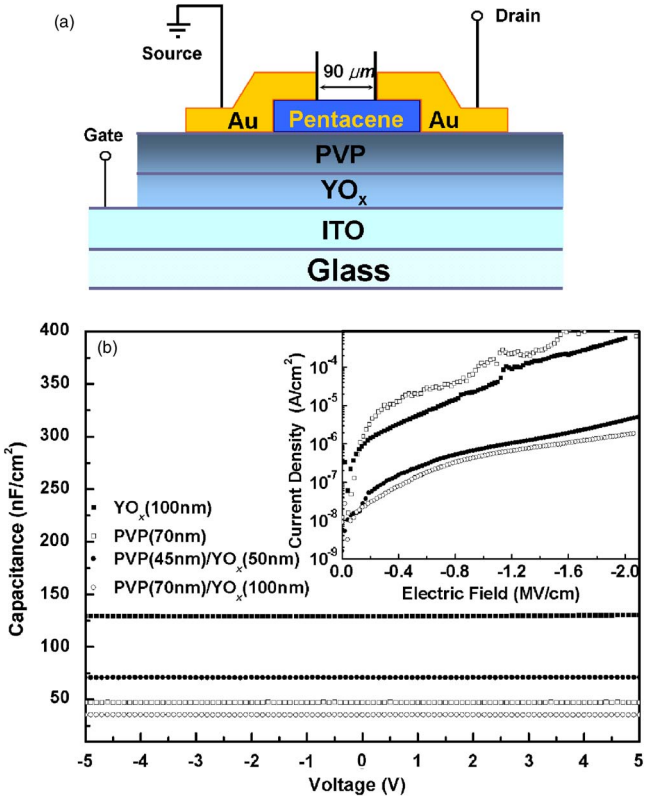

FIG. 1. (Color online) (a) A schematic cross-sectional view of our pentacene-based TFTs (channel length, L=90 μm; width, W=500 μm). (b) Plots of C-V and J-E (inset) characteristics measured from 300 μm diameter Au-dot/dielectric insulator/ITO structures. Chosen dielectrics were YO_x (100 nm), PVP (70 nm), and thin and thick double PVP/YO_x combinations (45 nm/50 nm and 70 nm/100 nm, respectively).

pacitance and strength of single (PVP, YO_x) and double (PVP/YO_x) insulators were measured. The capacitances of the YO_x (50 nm) and PVP (45 nm) single layers could not be measured because of their high leakage current but those of the 100 nm thin YO_x and 70 nm thin PVP single layer films were measured to be about 129 and 47.3 nF/cm^2, respectively. According to the capacitance data, the dielectric constant k of the YO_x and PVP films were estimated to be ~14.6 and 3.7, respectively. (According to the literature, stoichiometric crystalline Y_2O_3 does show k of 17–20 when the oxide films were annealed at an elevated temperature higher than 450 °C (Ref. 14) and that of PVP is similar to the previously reported values.[2,3]). Although the composition of our oxide deviated somewhat from the ideal bulk stoichiometry due to room temperature processing, our YO_x films exhibited quite a high dielectric constant. The thinnest double layer of PVP (45 nm)/YO_x (50 nm) exhibited quite a high capacitance value (70.8 nF/cm^2). Based on the following equation (1) and above dielectric constants of YO_x and PVP, the capacitance of thinnest double layer is worked out to be 57.3 nF/cm^2, because they are serially connected.

$$\frac{1}{C_{\text{total}}} = \frac{1}{C_{\text{PVP}}} + \frac{1}{C_{\text{YO}_x}}. \quad (1)$$

The theoretical capacitance value is somewhat different from our experimental one (70.8 nF/cm^2) and we cannot clearly explain the reason for the deviation, which thus remains to be a subject for further study. On the other hand, the measured capacitance of the PVP (70 nm)/YO_x (100 nm) combination, 35.2 nF/cm^2 was very close to that of serially connected double capacitors (34.6 nF/cm^2).

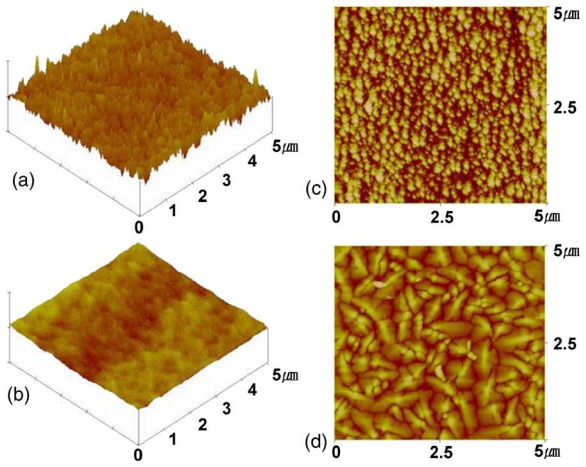

FIG. 2. (Color online) AFM images of (a) YO_x (100 nm) film deposited on ITO glass, (b) PVP (70 nm) layer coated on YO_x/ITO glass, (c) pentacene film deposited on the YO_x single layer, and (d) another pentacene film deposited on the PVP/YO_x double layer.

As shown in the J-E curve of Fig. 1(b) inset, the individual YO_x (100 nm) and PVP (70 nm) single layer films cannot properly function as a dielectric layer due to their very high leakage current. Of course, the 50 nm thin YO_x and 45 nm thin PVP single layer films showed much higher leakage current (not shown here). The J-E results from our thinnest double layer of PVP (45 nm)/YO_x (50 nm) provide us with one notable point. The double layer appeared to have quite a good dielectric strength of ~2 MV/cm based on our minimum leakage current standard of ~10^{-6} A/cm^2 even though its total thickness is only 95 nm (a 100 nm thick YO_x cannot match these characteristics as mentioned above). Since the leakage current paths of YO_x and PVP films are different from each other, it is likely that our organic-inorganic double layered films should have a much improved dielectric strength while the single layer films appeared rather vulnerable, failing easily under the same applied electric field.

Figures 2(a)–2(d) show the AFM surface images of the YO_x (a), PVP deposited on YO_x (b), pentacene deposited on YO_x (c), and finally the pentacene film grown on the PVP layer (d). The surface roughness of a 100 nm thick YO_x film on ITO glass was 1.83 nm, as shown in Fig. 2(a), which was improved to 0.62 nm [Fig. 2(b)] when a 70 nm thin PVP dielectric film was deposited by spin coating. Viscose PVP solutions must have filled up the valley regions on the YO_x surface during the spin coating. Besides improving the surface profile, it is also expected that our organic PVP layer changed the dielectric surface conditions from hydrophilic to more hydrophobic. As mentioned in the introduction, the hydrophobic surface states of organic dielectric film positively influence the growth of organic pentacene crystals while the hydrophilic surfaces cause negative effects.[15–18] This explains the fact that the pentacene film grown on the hydrophilic, rough YO_x resulted in very poor surface morphology [Fig. 2(c)] while the pentacene exhibited well-formed dendritic grains when grown on the hydrophobic, smooth PVP [Fig. 2(d)]. Consequently, our scheme of fabricating a pentacene TFT with a double layered dielectric with the PVP on top should be an effective strategy to achieve both a high-quality pentacene channel and a high-capacitance dielectric.

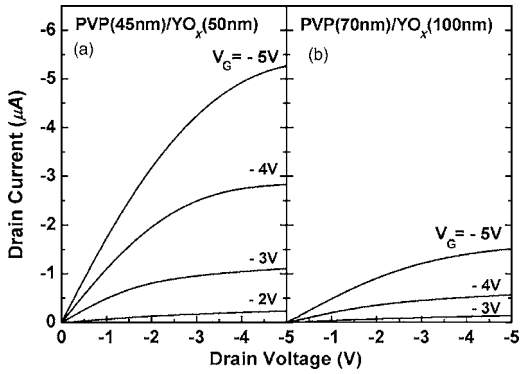

FIG. 3. Drain current-drain voltage (I_D-V_D) curves obtained from our pentacene-based TFTs with (a) PVP (45 nm)/YO_x (50 nm) and (b) PVP (70 nm)/YO_x (100 nm) dielectric combinations.

Figures 3(a) and 3(b) display the drain current-drain voltage curves (I_D-V_D) obtained from our pentacene-based TFTs with the PVP/YO_x double gate dielectric layers of two different thickness combinations: thin double (PVP/YO_x=45 nm/50 nm) and thick double (PVP/YO_x =70 nm/100 nm). Both types of devices demonstrated desirable TFT characteristics at an operating voltage lower than −5 V. Maximum saturation current of ~5.2 μA was achieved under a gate bias (V_G) of −5 V from the OTFT with the thin double dielectric layer while about 1.5 μA was achieved from the other OTFT with thick double dielectric, which must have a lower capacitance than the thin double dielectric.

Field effect saturation mobilities were determined from $\sqrt{-I_D}$ vs. V_G curves, as shown in Fig. 4. The pentacene TFT fabricated with the thin double dielectric layer has higher mobility of 1.74 $cm^2/V\,s$ than the device with the thick double dielectric, which also appears to have quite a good mobility of 0.67 $cm^2/V\,s$. The threshold voltages for the two pentacene TFTs were almost identical to be about −2.5 V and this result probably signifies that the PVP/pentacene-channel interface states for both TFTs are not much different, either.[19,20] According to the plots of $\log_{10}(-I_D)$-V_G of Fig. 4, the on/off current ratios for the two devices with thin double and thick double dielectrics were 2×10^4 and 4×10^3, respectively, while their subthreshold slope was again identical, about 0.6 V/decade. The performance of our devices with the double dielectric layers is comparable to those of previously reported pentacene TFTs with high-k dielectric films.[4–7] The field effect saturation mobility of our pentacene TFTs exhibits maximum of 1.74 $cm^2/V\,s$, which is much higher than any other corresponding values reported under low-voltage driving conditions.

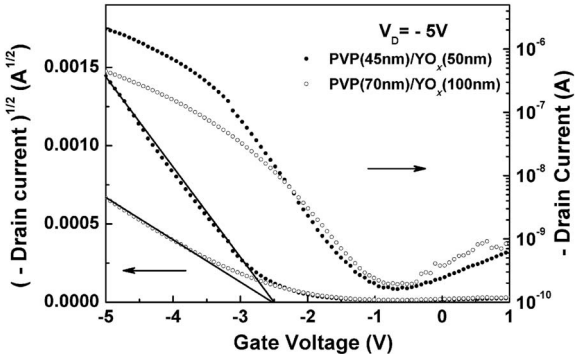

FIG. 4. $\sqrt{-I_D}$-V_G and $\log_{10}(-I_D)$-V_G plots obtained from our pentacene TFTs with PVP (45 nm)/YO_x (50 nm) and PVP (70 nm)/YO_x (100 nm) double dielectrics under a drain saturation condition (V_D=−5 V).

In summary, we have fabricated low-voltage pentacene TFTs, using PVP/YO_x double gate dielectrics. The thin PVP/YO_x double layers showed quite a good dielectric strength (~2 MV/cm) and decently high capacitance (~70.8 nF/cm^2) without much leakage. Our pentacene TFTs with the double dielectric layers displayed excellent maximum field effect mobility (1.74 $cm^2/V\,s$) because pentacene channel formation was controlled under optimal dielectric surface conditions: smoothness and hydrophobic states of PVP deposited on a thin high-k YO_x layer. We thus conclude that our PVP/YO_x double layer films are promising gate dielectric for low voltage high-mobility OTFTs.

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