Pentacene thin film transistors on inorganic dielectrics: Morphology, structural properties, and electronic transport

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The structural and transport properties of evaporated pentacene organic thin film transistors (TFTs) are reported, and they show the influence of the deposition conditions with different inorganic dielectrics. Dielectrics compatible with large area fabrication were explored to facilitate low cost electronics on glass or flexible plastic substrates. X-ray diffraction and atomic force microscopy show a clear correlation between the morphology and the structure of the highly polycrystalline films for all dielectrics investigated. The roughness of the dielectric has a distinct influence on the morphology and the structural properties, whereas the films on smooth thermal oxide are in general highly ordered and independent of the deposition conditions. The ordered films exhibit a ''thin film'' and a bulk phase, and the bulk phase volume fraction increases with the deposition temperature and the film thickness. Careful control of the deposition conditions gives virtually identical films on thermal oxide and silicon nitride dielectrics. The electronic properties of inverted staggered transistors show that the TFT mobility is correlated with the morphology and structure of the films. The TFTs exhibit very similar mobilities of ~ 0.4 cm^2/Vs and on/off ratios $>10^8$ on thermal oxide and silicon nitride. The impact of the dielectric on the device parameters of mobility, threshold voltage, and subthreshold voltage slope is discussed. Temperature dependent measurements of the mobility were performed to study the influence of traps on electronic transport. Bias stress experiments were carried out to investigate the stability of the TFTs, and to gain understanding of the transport mechanisms of thermally evaporated pentacene TFTs. © *2003 American Institute of Physics.* [DOI: 10.1063/1.1525068]

I. INTRODUCTION

Electronics based on organic and polymer materials have attracted much attention in recent years. The interest can be attributed to emerging demands in novel electronic devices like radio frequency tags (wireless transponders), smart cards, and display media (active and passive) on low cost and/or flexible substrates. Progress in this field has been sustained by improvements of the material properties[1–3] and in the development of processing techniques such as printing,[4–7] stamping, or other high volume parallel processing technologies. The processing techniques facilitate patterning of organic and inorganic materials without using standard photolithography. Therefore, most of the research has been driven by an interest in low cost electronics. Up to now amorphous and polycrystalline silicon have dominated low cost electronics due to low processing temperatures and the application of low cost substrates like glass or flexible foil, which facilitates scaling of the process to larger substrates.

Pentacene ($C_{22}H_{14}$) has demonstrated the highest hole and electron mobility of organic small molecules. The material exhibits a strong tendency to form highly ordered films which depend on the growth conditions and the substrate. Bulk single crystals are not favorable for low cost electronics, because the fabrication is time consuming and the crystals are small. Thin films are more favorable, because they can be fabricated on various low cost substrates. The hole mobility of thin film pentacene is close to the intrinsic transport limit of bulk single crystals, and thin film transistors (TFTs) with mobility of $\geqslant 1$ cm^2/Vs have been fabricated by several groups.[2,8–11] The mobility is therefore comparable with that achieved by amorphous silicon TFTs and hence pentacene TFTs might be considered for large area active matrix arrays. Promising methods for the fabrication of pentacene for low cost electronics on large areas are organic vapor phase deposition[12] and thermal evaporation.[8] In this article we focus on thermally evaporated pentacene.

The thermally evaporated material is polycrystalline and has large grains. The diameters are usually in the range of a few microns.[8,11,13] Despite the enormous progress in the realization of TFTs with good properties, the transport mechanism especially of polycrystalline films is not completely understood. Furthermore, most of organic TFTs so far have been fabricated on thermal oxide coated crystalline wafers. Thermal oxide on silicon wafers is a favorable substrate for the growth of pentacene, but for the applications intended silicon substrates are too small and expensive.

One of the requisites for the realization of low cost electronics is low cost substrates, for example, kapton (polyimide), polyethyleneterephtalate (PET), polyethersulfone (PES), or glass. To our knowledge, only a few research groups[8–11] have demonstrated pentacene TFTs on large area compatible dielectrics with high mobility. Attractive large area compatible inorganic dielectrics are sputtered Al_2O_3,

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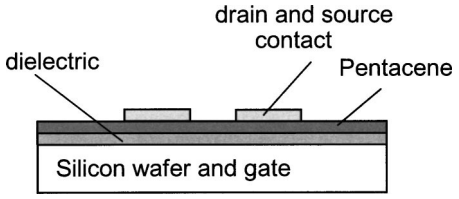

FIG. 1. Schematic of inverted staggered TFT test structure on highly doped *c*-Si wafer or glass substrate with a gate electrode. The gate dielectric was formed by thermal oxide, PECVD silicon nitride, or silicon oxide. The drain and source contacts were realized by evaporated gold.

sputtered silicon oxide or plasma-enhanced chemical vapor deposited (PECVD) silicon nitride, and silicon oxide. In this article we focus on a comparison of PECVD silicon oxide and silicon nitride dielectrics, because they are compatible with existing display technology.

Section II of the article contains a brief description of the film and device preparation. Section III discusses the material properties of pentacene films deposited under different conditions on various dielectrics. Section IV describes the device performance of TFTs on different dielectrics taking the morphology and the structural properties of the material into account. The morphology of the material is correlated with the mobility of the organic thin film transistors in Sec. IV A. In Sec. IV B the electronic transport of the pentacene TFTs is discussed with a comparison of TFTs on thermal oxide as the standard or reference dielectric, and TFTs on PECVD silicon nitride, which is a very promising dielectric for large area organic electronics. The temperature dependent mobility of the TFTs is compared for different dielectrics in Sec. IV C. The stability and the influence of bias stress on the behavior of the TFTs are discussed in Sec. IV D.

II. DEVICE PREPARATION

Bottom gate, inverted staggered transistor configurations were selected to evaluate different material compositions on silicon wafer and glass substrates, and are illustrated in Fig. 1. The highly doped wafer, upon which a 100 nm dielectric was grown, formed the gate electrodes for TFTs on silicon substrates. Samples on glass substrates had a metal gate electrode (Cr) with thickness of typically 100 nm. The roughness of the glass substrate (Corning 1737) is similar to that of a crystalline silicon wafer. The gate dielectrics were PECVD silicon oxide or silicon nitride. To improve the device performance of polycrystalline pentacene TFTs the dielectric can be treated by a self-assembled monolayer (SAM), which changes the surface wetting properties of the dielectric. Octadecyltrichlorosilane (OTS) is a promising SAM which has already been widely studied.[8] Monolayers of OTS on thermal oxide and PECVD silicon oxide were formed by dip coating the substrate into a solution of OTS diluted with toluene or hexadecane.

The pentacene films were deposited using a thermal evaporation system, keeping the temperature of the source between 285 and 325 °C. Films were prepared between room temperature (RT) and 110 °C substrate temperature using deposition rates in the range of 0.5–3.5 Å/s. We used 97% pure pentacene (Aldrich) and two times sublimation purified material for the depositions. The drain and source contacts were formed after thermal evaporation of pentacene using a shadow mask to form 100 nm thick gold drain and source contacts. The top contact structure is simple and helps ensure that the TFT measurements reflect the differences in the dielectrics rather than possible contact effects. Test structures with TFT lengths of 30–150 μm were fabricated, and the TFT width is in the range of 0.1–5 mm.

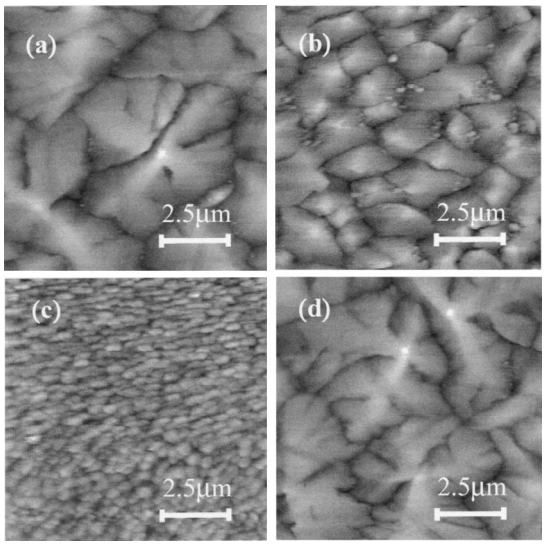

FIG. 2. Atomic force microscopy images of thermally evaporated pentacene films (50–70 nm) on inorganic dielectrics: (a) thermal oxide, (b) thermal oxide with OTS, (c) rough PECVD silicon nitride, and (d) smooth PECVD silicon nitride.

III. MATERIAL CHARACTERIZATION

The surface morphology of the pentacene films on different dielectrics was studied with atomic force microscopy (AFM) and x-ray diffraction (XRD). All pentacene films deposited on thermal oxide exhibit high structural order. The morphology of a pentacene film on thermal oxide prepared at elevated temperature is shown in Fig. 2a. The 50–70 nm thick film exhibits a dendritic structure, in which the size of the dendrites ranges from 3 to 6 μm. The corresponding x-ray diffraction pattern in Fig. 3 contains a series of $(00k')$ lines, indicating a highly textured material. The film consists mainly of one phase with a first order diffraction peak at 5.73° that corresponds to a lattice spacing of 15.5 Å. In the literature this is called the ''thin film phase'' and its structure has not been fully determined. The lattice spacing corresponds to a tilt of the molecules of 17.1° to the surface normal, assuming a triclinic single crystal structure.[11,12] The x-ray measurements exhibit a second $(00k)$ spacing from a second phase of the material, which is the crystal bulk phase of the material. The measured x-ray diffraction angle of 6.10° corresponds to a layer-by-layer spacing of 14.5 Å and a tilting of the molecules to the surface normal of 25.7°. Single crystalline pentacene exhibits a tilt of the *c* axis of the molecule of 25.2°, which is within experimental uncertainty.[14,15]

The morphology and the structural properties of pentacene films were studied as the substrate temperature, deposi-

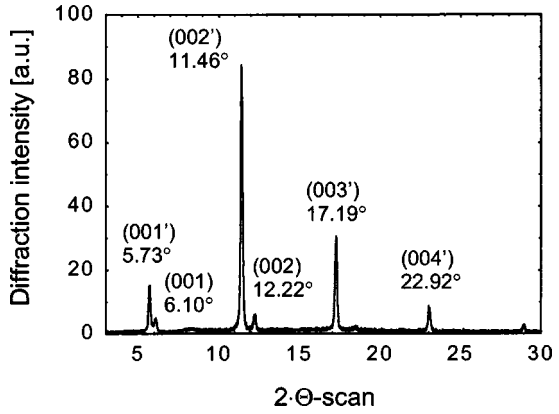

FIG. 3. X-ray diffraction pattern of thermally deposited pentacene film on a 100 nm thick thermal oxide film. The thickness of the pentacene film is approximately 70 nm. The deposition rate was kept constant (0.5 Å/s).

tion rate, and layer thickness were varied. Figure 4 shows the ratio of the two diffraction peaks at 5.73° (thin film phase) and 6.10° (bulk phase) as a function of the crystal size of pentacene films on thermal oxide. The substrate temperature was increased from room temperature to 90 °C and the deposition rate was 3.5 Å/s. Enhanced substrate temperatures lead to an increase of the crystal size from ~150 nm to ~5 μm. The ratio of the diffraction peaks changes as a function of the substrate temperature from <0.03 to >1. A further increase of the substrate temperature (to >90 °C) leads to no growth of pentacene on the substrate. The increase of the crystal size and the shift of the diffraction peaks from the thin film phase towards the bulk phase were also observed for other deposition rates and substrates. At reduced deposition rates, the transition from the growth to the nongrowth region shifts toward lower substrate temperature. Furthermore, large crystals can already be grown at lower substrate temperatures. The change of the ratio of the XRD intensities in Fig. 4 reveals that an increase of the substrate temperature results in a change of the volume fraction of the two-phase system. Therefore, the structure of the two-phase system (thin film phase and bulk phase) shifts towards the bulk phase for higher temperatures. However, the thin film and the bulk phase are both crystalline and highly ordered.

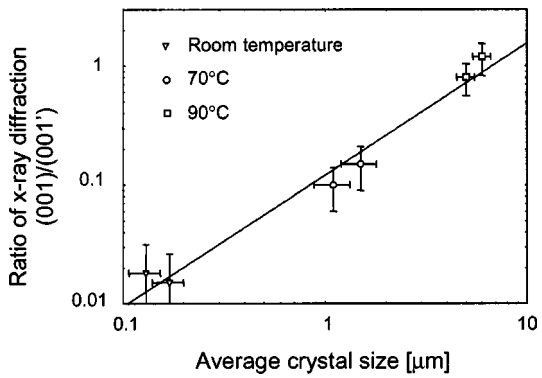

FIG. 4. Ratio of x-ray diffraction peaks (001)/(001′) of thermally evaporated pentacene films on thermal oxide. The thickness of the film is 200 nm and the substrate temperature was varied from room temperature to 90 °C.

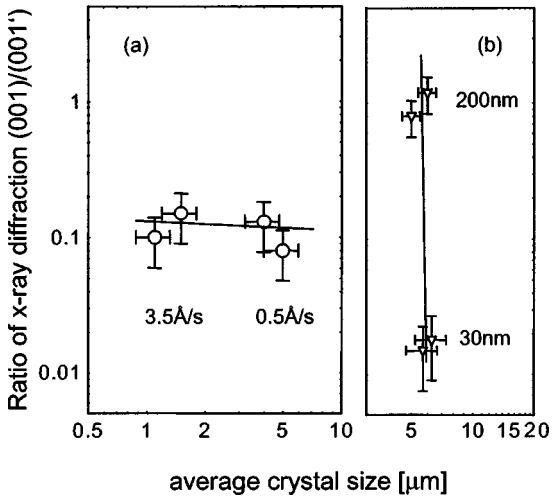

FIG. 5. Ratio of x-ray diffraction peaks (001)/(001′) of thermally evaporated pentacene films on thermal oxide. (a) Influence of the deposition rate; (b) influence of the layer thickness.

The influence of the deposition rate and the thickness of the film on the crystal size and the x-ray diffraction of the films are shown in Fig. 5. The size of the dendrites is enhanced as the deposition rate decreases, but the ratio of the diffraction peaks of the films remains nearly unchanged. This behavior occurs for deposition rates ranging from 0.5 to 3.5 Å/s and for film thickness up to 250 nm. However, an increase of the film thickness does not affect the size of the dendrites. Therefore the initial nucleation sites determine the morphology of the final layer and only the roughness of the pentacene films increases with an increase in film thickness. The x-ray diffraction of the film however shifts from the thin film phase towards the bulk phase of the material with an increase in thickness. The results indicate that a thin film layer of pentacene is grown at the interface of the dielectric and the channel. With an increase in thickness the structure of the film changes towards the bulk phase. However, the AFM measurements indicate that the morphology of very thin layers of pentacene is not characterized by a dendrite-like structure. Instead, a very thin layer grows as a continuous film, which changes to dendrite-like growth at a layer thickness of 5–15 nm. This is of particular interest because current transport of the TFT largely occurs in a thin layer at the interface.

When the thermal oxide is treated with an OTS monolayer, the crystals exhibit a reduced size of 1–2 μm. An AFM image of a pentacene film grown on an OTS treated substrate is shown in Fig. 2(b). The monolayer changes the surface properties of the thermal oxide to a more hydrophobic surface, as shown by the surface-wetting angle of 95°. The growth of pentacene on OTS is characterized by island formation but no dendrite-like crystal formation is observed. The x-ray diffraction pattern of pentacene films on OTS exhibits maxima at 5.74° and 6.11°, so the position of the diffraction maxima is unchanged. However, the XRD measurements indicate a change of the structural properties of the pentacene films due to OTS treatment. The crystalline bulk peak at 6.11° was increased for the OTS treated dielectrics, whereas the intensity was reduced for the thin film phase.

Therefore the growth process of pentacene is affected by the wetting properties of the dielectric. AFM images of very thin layers of pentacene on OTS treated substrates confirm these results.[16] In the case of OTS treated substrates the pentacene molecules prefer to grow more vertically rather than laterally like what is observed for hydrophilic substrates.

Figure 2(c) shows an atomic force image of a pentacene film grown on a 100 mn thick PECVD silicon nitride dielectric. The pentacene deposition rate was 0.5 Å/s and the substrate temperature was kept constant at 70 °C during deposition. Small crystals 100–200 nm in diameter characterize the morphology of the film. Changing the pentacene deposition conditions (substrate temperature and the deposition rate) leads to only minor changes of the morphology of the film. The results for these early PECVD silicon nitride dielectrics are evidently completely different from the results observed for thermal oxide [Fig. 2(a)]. The material is disordered without preferential orientation, since no x-ray diffraction pattern could be measured. AFM measurements of the silicon nitride dielectric itself showed that the dielectric has a peak-to-valley roughness of 5.5 nm [and root mean square roughness (rms) of 0.8 nm] on single crystalline wafers and an even more pronounced roughness of 9.5 nm (rms of 1.4 nm) on glass substrates. As might be expected, the roughness increased with the thickness of the dielectric. For comparison, the peak-to-valley (rms) roughness of our thermal oxide is 0.5 nm (0.15 nm). However, using the PECVD silicon nitride dielectric for amorphous silicon and polysilicon TFTs provides mobility of ~ 1 cm^2/Vs (Ref. 17) and >100 cm^2/Vs.[18]

To improve the growth of pentacene on the large area and/or low cost compatible substrate, we modified the fabrication process of the PECVD silicon nitride layer so that the surface of the dielectric becomes smoother.[13] In Fig. 2(d), shown is an AFM image of a pentacene film which was grown on a PECVD silicon nitride film with a 2.7–3.0 nm peak to valley roughness and 0.35 nm rms roughness. The smoother dielectric evidently results in greatly improved pentacene growth. We obtained the typical dendrite-like shape of pentacene prepared at elevated temperature. The same deposition conditions were used to grow the pentacene films in Figs. 2(a) and 2(d), and the film thickness was 50–70 nm in both cases. Virtually no difference in morphology could be observed for the film on thermal oxide [Fig. 2(a)] and on PECVD silicon nitride [Fig. 2(d)].

The morphology results are confirmed by measurements of the structure. The x-ray diffraction pattern of pentacene on smooth silicon nitride is shown in Fig. 6. A comparison of the diffraction patterns in Figs. 3 and 6 indicates that both films are highly ordered. Both films exhibit typical x-ray peaks at 5.74°, corresponding to the thin film phase, and a distinctly smaller peak at 6.10°, corresponding to the crystalline bulk phase of the material. A comparison of the third and the fourth order diffraction peaks indicates higher diffraction intensities for the pentacene film on the thermal oxide. At this point it is not clear whether the reduced peaks for the film on PECVD silicon nitride are due to the reduced long-range order of the film or due to uncertainties in the XRD measurement. Further work is required to quantify diffraction intensities for different films and substrates, but it is evident that very similar pentacene can be grown on the two dielectrics.

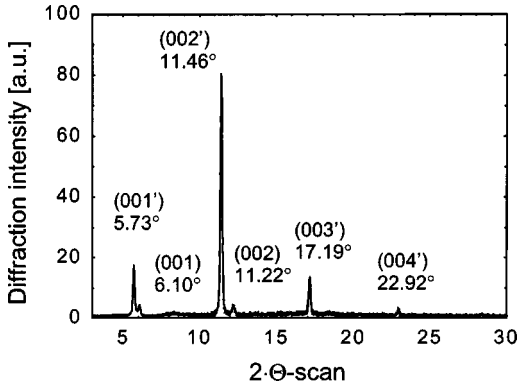

FIG. 6. X-ray diffraction pattern of thermal deposited pentacene film on a 100 nm thick amorphous silicon nitride film. The thickness of the pentacene film is approximately 70 nm. The deposition rate was kept constant (0.5 Å/s).

The morphology of pentacene films on PECVD silicon oxide is characterized by the formation of relatively small crystals with typical diameters of 1–2 μm. As growth proceeds, a transition is observed from the growth of individual crystals towards the formation of a continuous film.

In summary, material with similar morphology can be grown at different preparation conditions. At lower substrate temperatures (70 °C) a low deposition rate (0.5 Å/s) is required to grow material with large crystals ($\geqslant 5$ μm), whereas for higher substrate temperatures (90 °C) the deposition rate can be increased so large two-dimensional crystals will form. These observations indicate increased surface mobility of the material at higher temperature, which results in faster formation of crystals. Again, the thin film and crystalline phase are both polycrystalline and highly ordered. The structural properties of thin pentacene films are dominated by the thin film phase of the film. The change of the ratio of the XRD intensities in Figs. 4 and 5 reveals that an increase of the substrate temperature and film thickness results in a change of the volume fraction of the two-phase material. The composition of the two-phase material (thin film phase and bulk crystalline phase) shifts towards the crystalline phase for higher temperatures.

The substrate properties also strongly affect the morphology and the structural properties of pentacene films. This includes not only the physical (roughness) but also the chemical (surface wetting) properties of the dielectric. Therefore, the morphology and the structural properties of the films are determined by the physical and chemical properties of the dielectric. The properties of very thin films are dominated even more by the substrate and the surface properties and less by the deposition parameters.

IV. DEVICE CHARACTERIZATION

A. Influence of the dielectric on the mobility

The mobility of pentacene TFTs on different inorganic dielectrics is given in Fig. 7, and is correlated with the pen-

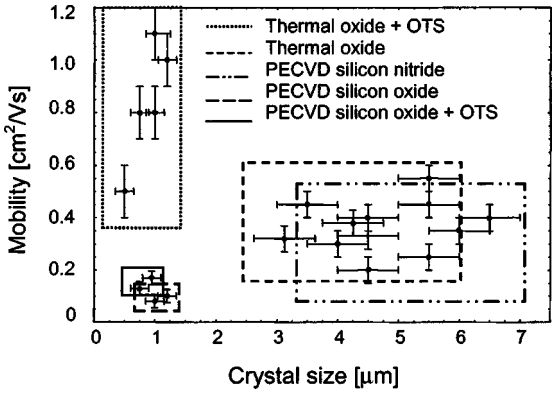

FIG. 7. Mobility of thermally evaporated pentacene thin film transistors on different inorganic dielectrics (thermal oxide with and without OTS, PECVD silicon oxide with and without OTS, and PECVD silicon nitride) as a function of the crystal size. The crystal size was determined by AFM measurements.

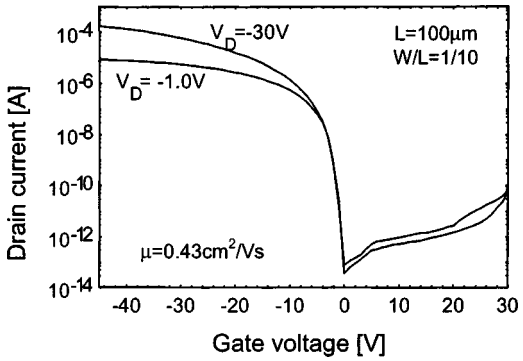

FIG. 8. Measured transfer curves of a pentacene TFT deposited on silicon nitride (100 nm) for $V_D=-1$ and -30 V. The pentacene film with thickness of approximately 70 nm was prepared at 70 °C substrate temperature at a deposition rate of 0.5 Å/s.

tacene crystal grain size. As a standard and reference dielectric we used silicon thermal oxide, because it is well known that oxidized silicon wafers are favorable substrates for the growth of pentacene. Many samples were measured and the boxes in Fig. 7 indicate the range of values obtained for the different dielectrics. The pentacene TFTs on thermal oxide deposited at 70 °C exhibit mobilities of the order of 0.2–0.6 cm^2/Vs and the size of the dendrites ranges from 2 to 6 μm. The mobility was extracted from fits to the saturation regime. The mobility in the linear region is typically 0%–20% lower than the saturation mobility. The corresponding AFM image is shown in Fig. 2(a) and the XRD pattern in Fig. 3. The on/off ratio of the TFTs is more than eight orders of magnitude. There is a small positive onset voltage of the drain current and a negative threshold voltage. A more detailed description of the TFT performance on thermal oxide is given elsewhere.[13]

When the thermal oxide is treated with an OTS monolayer, the mobility increases to $\sim$1.0 cm^2/Vs although the crystal size was significantly reduced to 1–2 μm, and the pentacene films on OTS barely exhibit dendrites. Transistors using OTS treatments exhibit a larger variation in mobility from run to run (0.5–1.4 cm^2/Vs) using the same preparation conditions, and this may be due to differences in monolayer formation. In general, all the TFTs exhibit variation in the device parameters from run to run even when using the same preparation conditions. The mobility and the on/off ratio of TFTs made on untreated dielectrics can be relatively well reproduced, whereas the threshold behavior of the devices is affected more by variations.

The TFT results for the smooth PECVD silicon nitride are similar to those of the untreated thermal oxide devices (see Fig. 7), and a typical TFT transfer characteristic is shown in Fig. 8. The mobility of the smooth PECVD silicon nitride TFTs varies between 0.2 and 0.55 cm^2/Vs, and the crystal size range is 3–7 μm. The transfer characteristics tend to be shifted toward more negative voltage, probably reflecting different charging of silicon nitride. The similarity in TFT properties mirrors the close similarity in morphology and structure of the pentacene on the two dielectrics, as discussed in Sec. III. Pentacene films on rougher silicon nitride have reduced mobility by a factor of $\sim$100, down to 10^{-3}–10^{-2} cm^2/Vs.

For pentacene TFTs on PECVD silicon oxide, the mobility and the crystal size are reduced to $\sim$0.07 cm^2/Vs and $\sim$1 μm, respectively (see Fig. 7). The use of OTS doubles the mobility to $\sim$0.18 cm^2/Vs. AFM measurements of the substrate indicate that the dielectrics are too rough to provide growth of larger dendrites. Nevertheless, the application of OTS leads to an improvement of the mobility by a factor of 2–3, which is similar to the improvements on thermal oxide substrates. The on/off ratio of the thin film transistors on thermal oxide (with and without OTS) and on PECVD silicon nitride was $>10^8$, whereas the on/off ratio of TFTs on PECVD silicon oxide (with and without OTS) was slightly reduced to $>10^7$. All the TFTs had similar off currents in the range of 1–10 fA/μm and these low values are limited by our measuring setup. Therefore, the geometry of the transistors and the on current of the TFTs partially determine the on/off ratio.

In general, the strong correlation between the morphology and the structural properties is reflected in device performance. The TFTs on thermal oxide and PECVD silicon nitride exhibit the same morphology, structural properties, and room temperature mobility. Decreasing the crystal size, as observed for the PECVD silicon oxide, reduces the mobility. In this case the reduction in crystal size seems to be attributable to the increased roughness of the dielectric. However, the surface wetting properties add another parameter, which significantly changes the growth process and the TFT performance. Consequently, OTS treated dielectrics exhibit two to three times higher mobility.

B. Comparison of pentacene TFTs on thermal oxide and PECVD silicon nitride

A typical transfer curve of a TFT on smooth PECVD silicon nitride is plotted in Fig. 8. The thickness of the dielectric is 100 nm and the thickness of the polycrystalline film is 70 nm. The surface analysis of the pentacene films by AFM showed large dendrites with diameters up to 5 μm. The transistor in Fig. 8 exhibits mobility of 0.43 cm^2/Vs using a transistor length of 100 μm and a W/L of 10, and the on/off

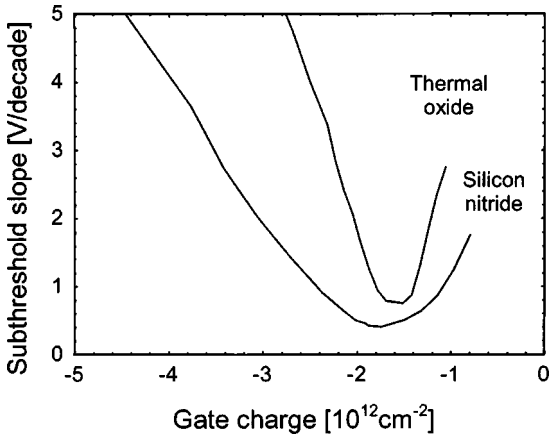

FIG. 9. Subthreshold slope of a pentacene TFT on thermal oxide and silicon nitride as a function of the gate charge. The pentacene film with thickness of approximately 70 nm was prepared at 70 °C substrate temperature at a deposition rate of 0.5 Å/s.

ratio of the TFT is $>10^8$. The leakage current is only slightly increased for higher positive voltages, so the on/off ratio remains higher than eight orders of magnitude over a wide range.

The subthreshold slope, which describes turn on of the TFTs, is another measure of device quality, and is defined by

$$S = \frac{\partial V_G}{\partial(\log I_d)}. \tag{1}$$

The subthreshold slope derived from the transfer characteristics of the TFTs is shown in Fig. 9. There is a minimum slope of 0.4 V/decade for the silicon nitride and a slope of 0.75 V/decade for the thermal oxide. In both cases the thickness of the dielectric is 100 nm, but the difference in threshold slope approximately reflects the different dielectric constant of thermal oxide and silicon nitride. We calculate a capacitance of 66 nF/cm^2 for the silicon nitride and 34 nF/cm^2 for the thermal oxide. Therefore, the subthreshold slope in charge/decade measured is equal for thermal oxide and silicon nitride devices. The results demonstrate that the slope of the thermal oxide is only slightly better than that of the PECVD material. It is known that the defect density of our silicon nitride is 4×10^{17} cm^{-3},[19] and therefore is more than five orders of magnitude higher than the defect density of thermal oxide. However, the subthreshold slope is apparently dominated by the material properties of the pentacene itself and less determined by defect states of the dielectric suggesting that trapping principally occurs in the organic material rather than in the dielectric.

The results for thermal oxide and PECVD silicon nitride are similar but the electronic transport of these polycrystalline films and the role of traps are not completely understood. In particular the influence of the grain boundaries and the nature of defects at the grain boundaries are still under discussion.[20,21] The experimental evidence clearly indicates that traps limit electronic transport,[22] and may be controlled by external influences.[23] Our experimental results for thermally evaporated pentacene films suggests that acceptor and donor states are required to describe electronic transport and

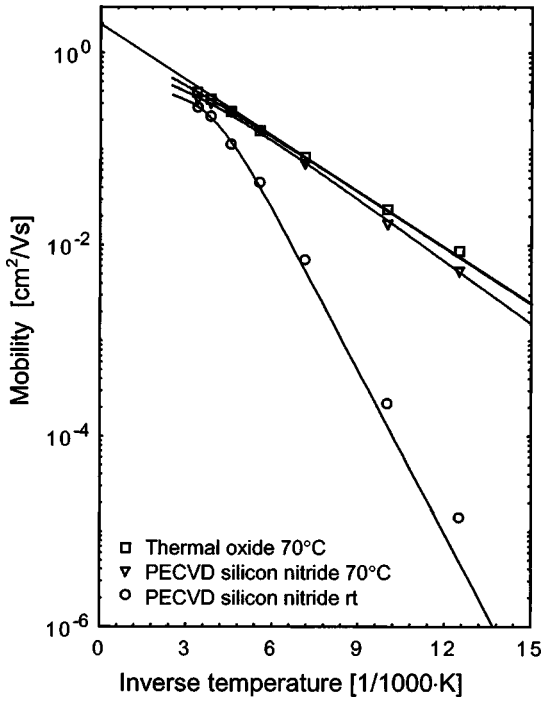

FIG. 10. Measured saturation mobility of pentacene TFTs prepared on thermal oxide (70 °C) and PECVD silicon nitride (RT and 70 °C).

potential barriers are not sufficient to describe the data.[21] With a decrease in crystal size the TFTs are less stable to atmosphere,[24] which can be explained by the penetration of oxygen. In order to understand the influence of oxygen and the nature of defects further studies are necessary.

C. Temperature dependent mobility

Further information about trap states near the valence band edge can be obtained by temperature dependent measurements of the TFT parameters. The temperature dependent mobility of TFTs on thermal oxide and PECVD silicon nitride is shown in Fig. 10. All three TFTs were exposed to air for a few weeks before performing the measurement and no specific precautions were taken to prevent the penetration of oxygen into the film. For the two films on thermal oxide and PECVD silicon nitride prepared at 70 °C we measured the mobilities at room temperature between 0.3 and 0.4 cm^2/V s. The saturation mobility for both these TFTs decreases with the temperature, and follows a very similar dependence. The TFT deposited at room temperature on silicon nitride has a stronger temperature dependence of its mobility.

The decrease in mobility is an indication of trap states near the band edge and shows that the Fermi energy does not reach mobile states. In contrast, in single crystal pentacene grown with extremely low levels of impurity, the mobility increased at low temperature and electronic transport was limited by phonon scattering rather than by trapping. For the polycrystalline films, we assume a distribution, $N_T(E)$, of traps above the mobile valence band states. The effective mobility is the mobility of free carriers reduced by the fraction of holes that are trapped,

$$\frac{\mu_{\text{eff}}}{\mu_0}=\frac{N_V}{N_V+N_{\text{TH}}}\approx\frac{1}{1+\dfrac{N_{\text{TH}}}{N_{V0}}\exp\left(\dfrac{E_F-E_V}{kT}\right)}, \tag{2}$$

where N_{V0} is the effective density of states at the energy, E_V, of the valence band edge, and E_F is the Fermi energy. N_{TH} is the number of trapped holes, determined by the distribution $N_T(E)$ and the Fermi energy.

A fit of the experimental data to Eq. 2[25] gives an activation energy of the hole concentration of 40 meV for the thermal oxide and 42 meV for the PECVD silicon nitride, and this is a measure of the trap distribution. It is therefore apparent that both films must have similar trap distribution. The activation energy is in good agreement with experimental data from space–charge limited current measurements based on pentacene films.[26]

The third curve in Fig. 9 corresponds to a pentacene film prepared at room temperature on top of a PECVD silicon nitride dielectric. In this case the room temperature mobility is slightly below 0.3 cm^2/Vs, similar to the other two films. X-ray diffraction measurements confirmed that all three films are highly ordered and primarily in the thin film phase. However, the morphology of the films is different, in that pentacene crystals prepared at room temperature are distinctly smaller than crystals grown at elevated temperature on thermal oxide and PECVD silicon nitride. The mobility of the film prepared at room temperature exhibits stronger temperature dependence, with a Fermi level of 110 meV from E_V, indicative of a broader distribution of traps. The different morphology of the film possibly allows greater penetration of oxygen and leads to the creation of more defects in comparison to in films with large crystals.

The experimental data are in good agreement with numerical calculated data of polycrystalline pentacene TFTs recently published by Völkel *et al.*[27] The calculations were based on an exponential distribution of defects states in the band gap. To describe the I/V characteristic of the TFTs at room temperature a narrow distribution of donors very close to the valence band and a broad distribution of acceptors have to be considered. A more detailed description of the model and the influence of the defects on device performance will be given in Ref. 28. A comparison between experiment and simulation reveals that oxygen leads to the generation of acceptor-like states deeper in the gap band.

D. Influence of bias stress on device behavior

The threshold voltage, and in particular its shift with prolonged application of gate bias stress, is an important parameter for the characterization of thin film transistors. It is well know that bias stress shifts the threshold voltage in both organic and inorganic TFTs.[13,29–31] The shift in threshold voltage for amorphous and polycrystalline silicon TFTs has been extensively investigated.[29,30] Its effect can arise from slow trapping in the dielectric and/or surface states at the semiconductor/dielectric interface, or the creation of defects in the semiconductor. So far few papers have been published that address these issues in pentacene.[13,31]

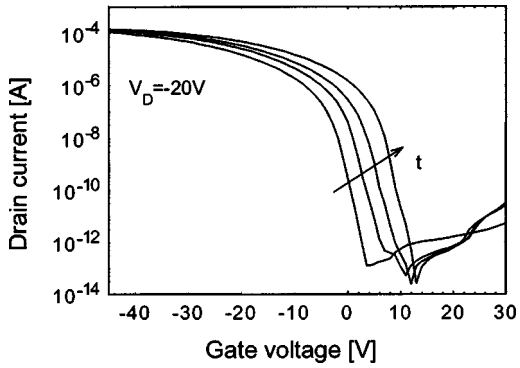

FIG. 11. Measured transfer curves of a pentacene TFT deposited on silicon nitride (100 nm) for $V_D=-20$ V. The transfer curve was measured after 0, 10, 30, and 90 min gate bias stress of $V_G=10$ V.

Our stress measurements are made under ambient conditions and the measuring cycle of the transfer characteristics takes 350 s using voltage steps of 1 V and a delay between measuring points of 5 s. The transfer curves of a TFT on smooth PECVD silicon nitride are plotted in Fig. 11 after various periods of positive gate bias stress. During an interval in the stress and the measurement sequence the drain voltage is fixed at $V_D=-20$ V. The arrow in Fig. 11 indicates the increase of stress time from 0 (unstressed) to 10, 30, and 90 min, respectively, and these cause a shift in threshold voltage of about 8 V. The mobility, the on/off ratio, and the subthreshold slope are minimally affected by gate bias stress. Figure 12 plots the shift of the threshold voltage for different drain voltages and stress times, and includes data for negative gate bias stress. Positive bias stress moves the threshold voltage towards positive voltages, whereas for negative gate stress the threshold voltage shifts towards negative threshold voltages.

The threshold voltage increases over time but with a nonlinear dependence, and the shift increases with stress bias. There is a more pronounced shift of V_T for positive gate voltages, but the form of the data for negative bias is otherwise rather similar. With high positive bias stress ($V_G=30$ V), the subthreshold slope is also affected, and changes from 0.5 to more than 1 V/decade, while the mobility and the on/off ratio remain unchanged. The stress measurements

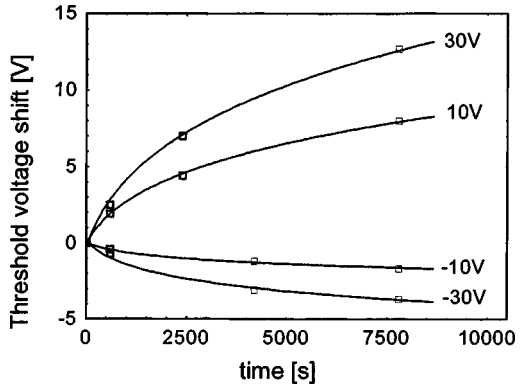

FIG. 12. Measured shift of the threshold voltage of a pentacene TFT deposited on amorphous silicon nitride (100 nm) under different gate bias stress conditions. The TFT was stressed for 0, 10, 30, and 90 min.

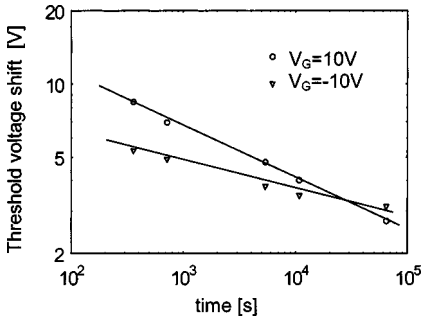

FIG. 13. Measured recovery of the threshold voltage of a pentacene TFT on thermal oxide. The TFT was stressed at $V_G = -10$ and 10 V for 90 min.

were repeated at reduced drain voltages, and we observed a weaker shift of the threshold voltage at lower bias voltages.

Equivalent measurements of pentacene TFTs on thermal oxide were made and we find similar bias stress behavior. Specifically, for TFTs on thermal oxide, a gate bias stress of $V_G = 10$ and 30 V (off state) leads to a shift of the threshold voltage of $\Delta V_T = 8.5$ and 14.5 V, respectively, very similar to the observations in Fig. 11. Stressing the TFT in the on state leads to a reduced shift towards negative voltages.

The change in threshold voltage of other TFTs is described by the following empirical equation:[29]

$$\Delta V_T \propto |V_G|^{\beta} t^{\gamma} \exp\left(-\frac{E_A}{kT}\right), \tag{3}$$

where V_G and t correspond to the gate voltage and the stress time, and β and γ are stretching factors. The third term in Eq. 3 describes the temperature dependence, but since our measurements are made at room temperature, this term is not investigated. The pentacene shifts in threshold voltage are described quite well by Eq. 3, and the fits are shown in Fig. 12. With positive gate voltages the stretching factors are $\beta = 0.35$ and $\gamma = 0.22$, and in the case of negative bias stress, the stretching factors are $\beta = 0.75$ and $\gamma = 0.06$. The increases of threshold voltage in Fig. 12 can be described by the change of gate voltage from $V_G = 10$ to 30 V.

The recovery kinetics after stressing a TFT was also studied. The recovery of the threshold voltage of a TFT on thermal oxide is plotted in Fig. 12, and similar data are obtained for the silicon nitride dielectric. After stressing the sample at $V_G = \pm 30$ V for 90 min, the gate and the drain voltages are switched off and left floating for different periods of time up to 18 h. The transfer curves of the TFT were measured periodically to obtain the threshold voltage, and the results are shown in Fig. 13 for positive and negative bias stress. The recovery follows a power law time dependence and takes a few days at room temperature to completely recover the original conditions. The gate and the drain were grounded during the recovery experiment.

The shift in threshold voltage under bias stress, and its recovery, are very similar for thermal oxide and PECVD silicon nitride dielectrics. These results suggest that the pentacene material, rather than the dielectric, determines the TFT properties. In general, the shift of bias stress threshold voltage may be due to charge trapping in the dielectric, trapping and slow release of carriers in existing deep states in the semiconductor (bulk or interface), or a reversible structural change in the semiconductor that creates new traps. The observation of very similar shifts for both the nitride and oxide dielectrics suggests that charge trapping in the dielectric is not the origin of the effect. The long recovery time and the fact that neither the measurement cycle nor brief illumination gives any observable change in the threshold voltage suggests that trapping in existing states is also unable to explain the shift of threshold voltage.

Hence, the results suggest that the shift of threshold voltage may be due to a reversible structural change in the pentacene film, which is induced by the accumulation of either holes or electrons and which creates deep localized states near the interface. The magnitude of the shift requires a state density of more than $10^{12}/\text{cm}^2$, and the defects need to be acceptor like for positive bias stress and donor-like for negative bias stress. The bias measurements therefore underscore that donor- and acceptor-like states are needed to describe the behavior of polycrystalline pentacene TFTs. Further studies are needed to confirm that structural changes in the pentacene are indeed the origin of the shift of threshold voltage and to identify the defects.

V. CONCLUSIONS

The structural and transport properties of polycrystalline pentacene on different dielectrics have been investigated. The films were thermally deposited on thermal oxide (with and without OTS), PECVD silicon nitride, and silicon oxide (with and without OTS). The material consists of two phases, a thin film and a bulk crystalline phase. The composition tends towards the crystalline phase and the formation of larger crystals at higher deposition temperature. The structural properties of the films are closely correlated with the morphology for each dielectric investigated. The growth of pentacene on silicon nitride is largely determined by the roughness of the underlying film. By preparing smooth silicon nitride films we have improved the structural properties of the pentacene film so that it is equivalent to films deposited on thermal oxide. The surface chemistry also has a strong influence on the growth of the material and electronic properties. Changing surface wetting more towards a hydrophobic surface by using OTS leads to the growth of smaller crystals but the mobility is improved by a factor of 2–3 for thermal oxide and PECVD silicon oxide.

PECVD silicon nitride appears to be a good candidate for large area compatible and inorganic dielectrics, because the fabrication process is an already established and well-known process. TFTs on thermal oxide and PECVD silicon nitride exhibit mobilities of around 0.4 cm^2/Vs and on/off ratios of more than eight orders of magnitude. The morphology and the structural properties of pentacene films on thermal oxide and PECVD silicon nitride are very similar. Even the trap distribution determined for TFTs on the different dielectrics is similar. Investigations of the subthreshold slope also revealed that the material itself determines transport and that trapping in the dielectric is only a minor effect. Investigations of TFTs under stress conditions exhibit a distinct shift of threshold voltage under gate bias stress, with similar

properties for both oxide and nitride dielectrics. The measurements suggest that the shift of threshold voltage is due to a reversible structural change in the pentacene film that creates deep localized states.

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